Stereo CMOS bitstream DAC for digital audio systems

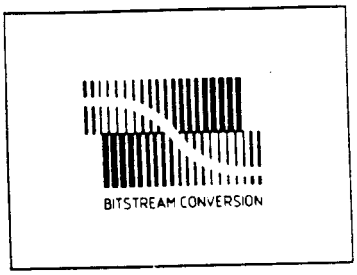
SAA7322/SAA7323

FEATURES

- I²S data input
- 3-stage digital filter incorporating F.I.R. filter, linear interpolator and sample-and-hold
- 2nd order noise shaper to improve analog performance
- 16-bit resolution from a bitstream conversion DAC, using switched capacitor integrator
- 3rd order low-pass filter to reduce out-of-band noise
- −12 dB attenuation, de-emphasis and mute control
- TTL compatible input/outputs

GENERAL DESCRIPTION

The SAA7322/7323 (DAC3) is a complete monolithic stereo CMOS 16-bit input bitstream conversion digital-to-analog converter designed for use in digital audio systems. The device is a replacement for the SAA7320, offering improved "idle pattern" performance at low-levels. The SAA7322 is a lower performance version of the SAA7323.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	20	35	mA
I_{DDD}	digital supply current		–	40	85	mA
DR	dynamic range SAA7322 SAA7323	note 1	 – 93	 93 –	 – –	 dB dB
THD+N	total harmonic distortion plus noise SAA7322 SAA7323	note 1	 – –	 −88 –	 – −90	 dB dB
f_{XTAL}	operating crystal frequency		8	11.2896	12.3	MHz
T_{amb}	operating ambient temperature range SAA7322 SAA7323		 −10 −40	 – –	 +70 +85	 °C °C

Note to the quick reference data

1. Output characteristics measured with external components shown in Fig.10. Sample rate = 44.1 kHz.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7322GP	44	QFP	plastic	SOT205AG
SAA7323GP	44	QFP	plastic	SOT205AG

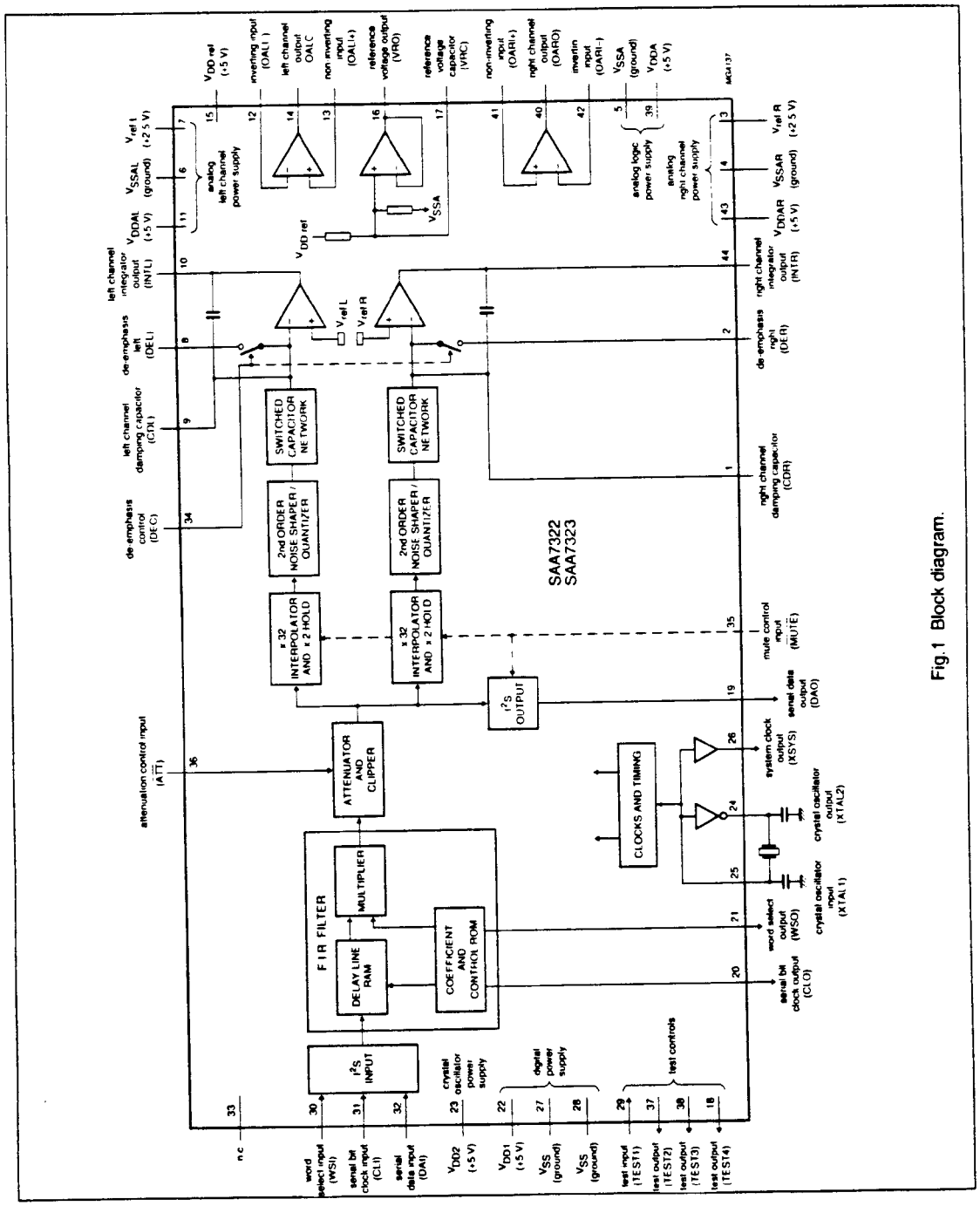


Fig.1 Block diagram.

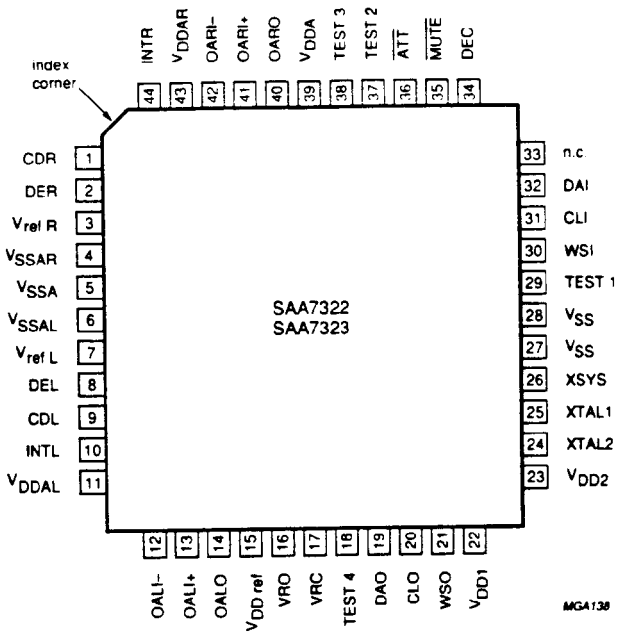


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
CDR	1	damping capacitor for the right channel switched-capacitor integrator
DER	2	connection to the de-emphasis switch in the right channel integrator
V_{refR}	3	reference voltage input for the analog channel ground (normally connected to VRO)
V_{SSAR}	4	ground connection for the analog right channel
V_{SSA}	5	ground connection for logic in the analog section
V_{SSAL}	6	ground connection for the analog left channel
V_{refL}	7	reference voltage input for the analog left channel ground (normally connected to VRO)
DEL	8	connection to the de-emphasis switch in the feedback of the left channel integrator
CDL	9	damping capacitor for the left channel switched-capacitor integrator
INTL	10	output from the left channel switched-capacitor integrator. Internal capacitor (85 pF typ.) connected to CDL
V_{DDL}	11	+5 V supply voltage for the analog left channel
OALI−	12	inverting input to the left channel low-pass filter operational amplifier
OALI+	13	non-inverting input to the left channel low-pass filter operational amplifier

SYMBOL	PIN	DESCRIPTION
OALO	14	output from the left channel operational amplifier
V_{DDref}	15	+5 V supply voltage for the reference voltage generator
VRO	16	internal reference voltage output (+2.5 V typ.)
VRC	17	internal reference voltage high impedance node requiring an external smoothing capacitor
TEST4	18	test output 4: pin should be left open-circuit
DAO	19	I²S serial data output is a 16-bit linear two's-complement PCM signal at a data rate of 176.4 kHz (typ.) formatted in accordance with I²S . After 4 x upsampling by the digital filter this signal is output so that an external DAC could be used; combined with CLO and WSO it can be considered as a master transmitter
CLO	20	I²S serial bit clock output, f_{CLKO} = 5.6448 MHz (typ).
WSO	21	I²S word select output 176.4 kHz (typ).
V_{DD1}	22	+5 V supply voltage for the digital section
V_{DD2}	23	+5 V supply voltage for the crystal oscillator
XTAL2	24	drive output to clock crystal
XTAL1	25	input from crystal oscillator or external clock input 11.2896 MHz (typ.)
XSYS	26	buffered output from crystal oscillator
V_{SS}	27, 28	ground connection for the digital section
TEST1	29	test input 1, pin should be connected to ground
WSI	30	I²S word select input, 44.1 kHz (typ) WSI together with CLI, is used to clock the I²S serial data input (DAI) and synchronize the main timing chain
CLI	31	I²S serial bit clock input, f_{CLKI} = 2.8224 MHz (typ).
DAI	32	I²S serial data input is a 16-bit linear two's-complement PCM signal formatted in accordance with I²S. If more than 16 bits are supplied then the least significant bits (LSBs) will be truncated
n.c.	33	not connected
DEC	34	de-emphasis control input switches an extra external capacitor network into both the analog left and right channel integrator feedback
MUTE	35	when active LOW this Schmitt trigger control input will force the interpolator data input to zero. It will also force the I²S data output (DAO) to zero
ATT	36	when active LOW this control input provides −12 dB attenuation to the analog output amplitude
TEST2	37	test output 2, pin should be left open-circuit
TEST3	38	test output 3, pin should be left open-circuit
V_{DDA}	39	+5 V supply voltage for logic in the analog section
OARO	40	output from the right channel operational amplifier
OARI+	41	non-inverting input to the right channel low-pass filter operational amplifier
OARI−	42	inverting input to the right channel low-pass filter operational amplifier
V_{DDAR}	43	+5 V supply voltage for the analog right channel
INTR	44	output from the right channel switched-capacitor integrator. Internal capacitor (85 pF typ.) connected to CDR

FUNCTIONAL DESCRIPTION

General

The SAA7322/7323 CMOS DAC heavily oversamples to several MHz (256 x the sampling frequency f_s), so that the band-limiting filters required for waveform smoothing and out-of-band noise reduction are mainly digital. In addition to the digital filters, the circuit contains active components for analog post filtering. In most applications very few external components are required. An output after the 4 x upsampling filter allows the circuit to be used as an interface between the decoder and external DAC in high-performance compact disc systems. The device requires only one +5 V supply; the required reference voltage is generated internally.

Separate supply pins for each of the bitstream conversion DACs achieves high performance signal-to-noise ratio and channel separation.

There is no phase delay between the two analog outputs despite the fact that the upsampling filter structure is multiplexed between the two data channels.

Oversampling digital filter

This is a 3-stage digital filter

- The first stage provides 4 x oversampling to 176.4 kHz using a 128-tap F.I.R. low-pass filter. Data is stored in a cyclic RAM, the filter coefficients in a ROM and the convolutions are performed using an array multiplier.
- The second stage is a 32 x oversampling linear interpolator.
- The third stage provides 2 x upsampling using a sample-and-hold, giving a total of 256 x upsampling (11.2896 MHz).

The first stage oversamples to 176.4 kHz with a band-pass ripple of ±0.035 dB and a stop-band attenuation of –60 dB above 24.2 kHz. It also contains frequency response compensation for the interpolator/analog post-filtering roll-off and coefficient scaling to prevent overflow in the noise shaper.

The characteristics of the F.I.R. filter are shown in Fig.9.

Switched-capacitor DAC

The digital-to-analog conversion is achieved with a bitstream conversion DAC oversampled to 256 f_s with second-order noise shaping performed digitally to give a 1-bit Pulse Density Modulated (PDM) code. Integral with the actual bitstream conversion converter is a first-order low-pass filtering action which reduces the total HF noise power.

A switched capacitor technique is used for the bitstream conversion DAC which converts the PDM stream to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of a first-order filter. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure. The output slew rate of this filter is chosen so that the operational amplifiers always remains within its high gain linear region.

An internally generated out-of-band dither signal is used to suppress audible idling patterns in the noise shaper at low signal levels. This signal is injected digitally into the x 32 upsampling interpolator at a frequency of 352.8 kHz and a level of –20 dB.

Attenuation

Attenuation is controlled by the ATT input at pin 36. This input will allow an attenuation of the analog output amplitude by 12 dB during track search.

De-emphasis and low-pass filter

Extra on-chip analog circuitry provides post filtering:

- Input DEC (pin 34) switches an extra external capacitor network into both the left and right channel analog integrator feedback to control roll-off. Output from the right channel switched-capacitor integrator (INTR) is available at pin 44. Output from the left channel switched-capacitor integrator (INTL) is available at pin 10.
- A low-pass filter, for further attenuation of out-of-band noise, can be constructed using the internal CMOS operational amplifiers. The digital filter contains compensation for a third-order Butterworth filter with a –3 dB cut-off at 60 kHz.

I²S serial interface

The SAA7322/7323 has two I²S ports incorporated; DAI (pin 32) and DAO (pin 19).

- DAI receives data from the compact disc decoder IC (or any 16-bit 44.1 kHz I²S source).
- DAO transmits the 4 x oversampled data to an external DAC.

The 'slave' receiver requires a serial bit clock input (CLI; pin 31) and a word select input (WSI; pin 30). To ensure that the filter is 'in-phase' with the input, the main timing chain

is automatically synchronized to the incoming word select signal. The frequency of the data must also be synchronized to the filter by:

- the source supplying the 11.2896 MHz system clock via crystal oscillator input (XTAL1; pin 25).

or

- SAA7322/7323 supplying the system clock to the source via XSYS (pin 26).

The SAA7322/7323 will use only the 16 most significant bits of input data even though the I²S format allows a variable word length (see Fig.4).

The 'master' transmitter supplies bit clock, word select and data signals for the 4 x upsampled output (see Fig.5).

Conversion path

The data conversion path is shown in Fig.3. As both paths are identical only one path is shown. The data flow is in a serial format up to the linear interpolator stage and then separated into two channels.

A recommended system application diagram of the SAA7322/7323 is shown in Fig.10.

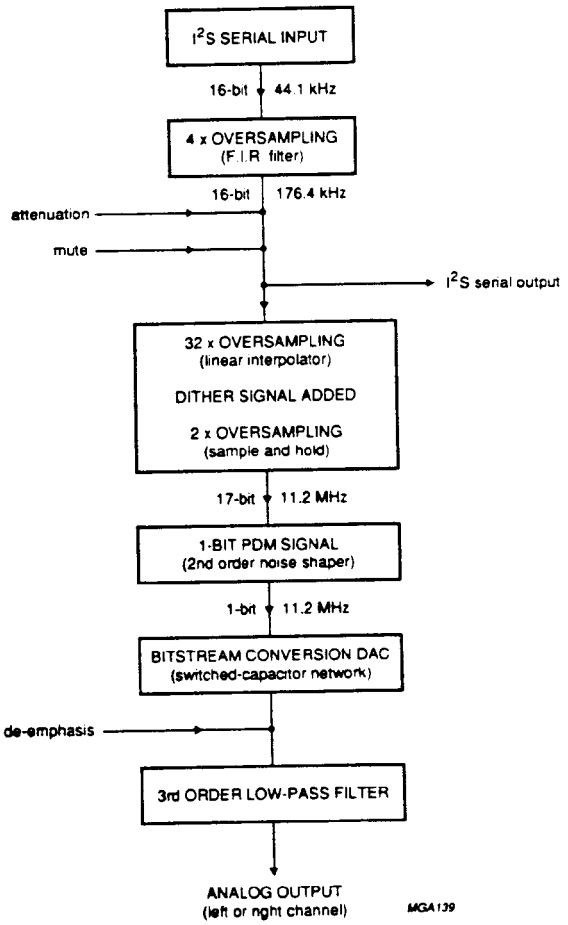


Fig.3 Flow diagram of SAA7322/7323 data conversion path (one channel).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	V_{DD}+0.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD}+0.5	V
I_O	DC output sink/source current		–	±25	mA
$I_{DD\ SS}$	total DC current V_{DD} or V_{SS}		–	±0.5	A
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range				
	SAA7322		−10	+70	°C
	SAA7323		−40	+85	°C
V_{es}	electrostatic handling	note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Suppy						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	20	35	mA
I_{DDD}	digital supply current		–	40	85	mA
Analog part						
REFERENCE VOLTAGE SOURCE VRC						
V_{refC}	high impedance reference voltage level		–	2.5	–	V
Z_{refO}	reference voltage output impedance		–	2	–	Ω
OUTPUTS OALO AND OARO (NOTES 1 AND 2)						
$V_{O\ RMS}$	output level (RMS value)	note 3; 0 dB	0.8	0.9	1.0	V
CHM	channel matching	note 4	–	–	±0.25	dB
OUTPUT PERFORMANCE (NOTE 1)						
DR	dynamic range SAA7322 SAA7323		 – 93	 93 –	 – –	 dB dB
THD+N	total harmonic distortion plus noise SAA7322 SAA7323	at 0 dB/1 kHz	 – –	 –88 –	 – –90	 dB dB
	digital silence		–	–96	–	dB
α	channel separation	at 1 kHz	–	90	–	dB
SVRR	supply voltage rejection ratio to V_{DD}		–	60	–	dB
L	linearity	–60 to –100 dB	–	±2	–	dB
Digital part						
INPUTS WSI, CLI, DAI, DEC AND ATT						
V_{IL}	LOW level input voltage	note 5	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 5	2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	note 6	–10	0	+10	μA
C_I	input capacitance		–	–	10	pF
MUTE (Schmitt trigger)						
V_{IL}	LOW level input voltage	note 5	–0.5	–	1.8	V
V_{IH}	HIGH level input voltage	note 5	3.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	note 6	–10	0	+10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance		–	–	10	pF
XTAL1 (external clock only)						
V_{IL}	LOW level input voltage	note 5	−0.5	–	1.5	V
V_{IH}	HIGH level input voltage	note 5	3.5	–	V_{DD} to 5 V	V
I_{LI}	input leakage current	note 6	−10	0	+10	µA
C_I	input capacitance		–	–	10	pF
OUTPUTS DAO, CLO, WSO AND XSYS						
V_{OL}	LOW level output voltage	note 5; I_{OL} = 400 µA	−0.5	–	+0.4	V
V_{OH}	HIGH level output voltage	note 5; I_{OH} = 20 µA	2.4	–	V_{DD}+0.5	V
C_L	load capacitance		–	–	35	pF
Crystal oscillator (input XTAL1, output XTAL2) (see Fig.8)						
f_{XTAL}	crystal operating frequency		8	11.2896	12.3	MHz
gm	mutual conductance	at 100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	G_v = gm x R_O	3.5	–	–	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 6	−10	–	+10	µA
Timing						
EXTERNAL CLOCK INPUT						
XTAL1						
f_{CLK}	input frequency	f_s x 256	8	11.2896	12.3	MHz
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
t_{HIGH}	input HIGH time	relative at 1.5 V to clock period	45	–	55	%
SYSTEM CLOCK OUTPUT XSYS (NOTE 8)						
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
t_{HIGH}	input HIGH time	note 9; relative at 1.5 V to clock period	45	–	55	%
I²S TIMING; RECEIVER CLOCK INPUT CLK_I (SEE FIG.6)						
t_{CLK}	input clock period		320	354	1000	ns
t_{CLKH}	input clock time HIGH		112	–	–	ns
t_{CLKL}	input clock time LOW		112	–	–	ns
Data input WSI and DAI						
$t_{SU\,DAT}$	data set-up time		40	–	–	ns
$t_{HD\,DAT}$	data hold time		40	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMITTER (SEE FIG.7)						
clock output CLO						
t_{CLK}	output clock period		–	$2/f_{CLK}$	–	ns
t_{CLKH}	output clock time HIGH		60	–	–	ns
t_{CLKL}	output clock time LOW		60	–	–	ns
Word select WSO						
$t_{SU\ DAT}$	data set-up time		40	–	–	ns
$t_{HD\ DAT}$	data hold time		40	–	–	ns
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
Data output DAO						
$t_{SU\ DAT}$	data set-up time		40	–	–	ns
$t_{HD\ DAT}$	data hold time		40	–	–	ns
t_r, t_f	input rise and fall time	note 7	–	–	20	ns

Notes to the characteristics

1. Output characteristics measured with external components shown in Fig.10. Sample rate = 44.1 kHz.
2. Maximum load on INTL, INTR (excluding feedback) is 10 kΩ, 20 pF to V_{ref}. Dynamic output impedance is typ. 150 Ω (open loop).
   Maximum load on OALO, OARO (excluding feedback) is 3 kΩ, 200 pF. Dynamic output impedance is typ. 100 Ω (open loop).
3. Output level changes linearly with clock frequency.
4. With matched external components.
5. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
6. $I_{LI\ min}$ and $I_{LO\ min}$ measured at V_I = 0 V; $I_{LI\ max}$ and $I_{LO\ max}$ measured at $V_I = V_{DD}$.
7. Reference levels = 0.8 V and 2 V.
8. Output times are measured with a capacitive load of 35 pF.
9. t_{HIGH} valid only when used with XTAL.

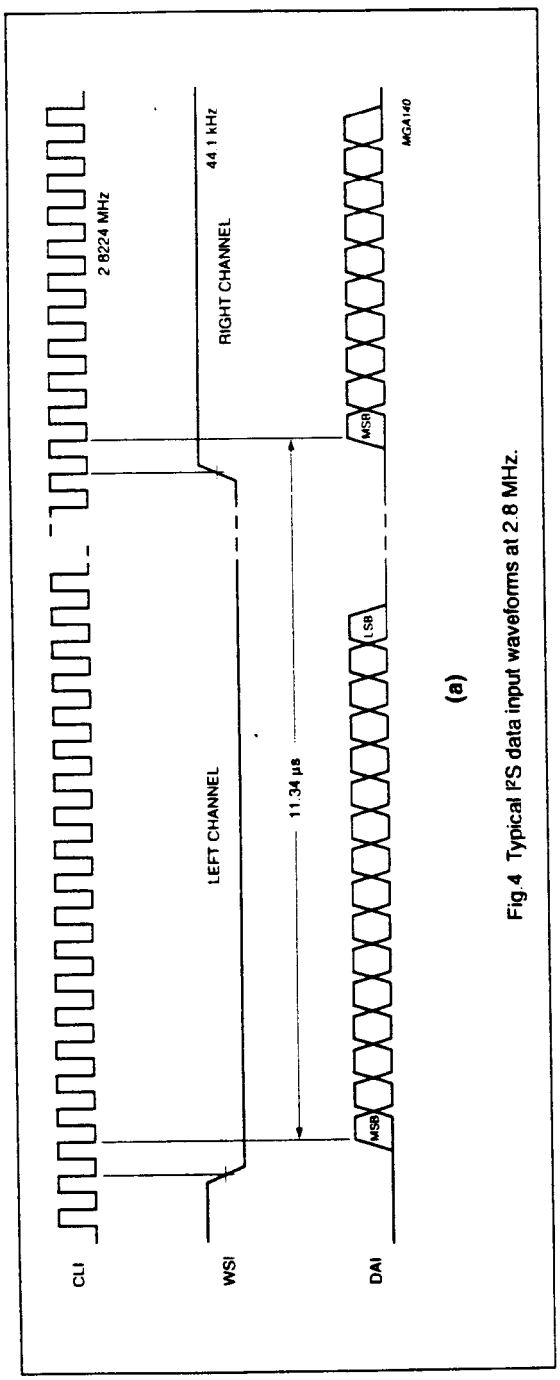


Fig.4 Typical I²S data input waveforms at 2.8 MHz.

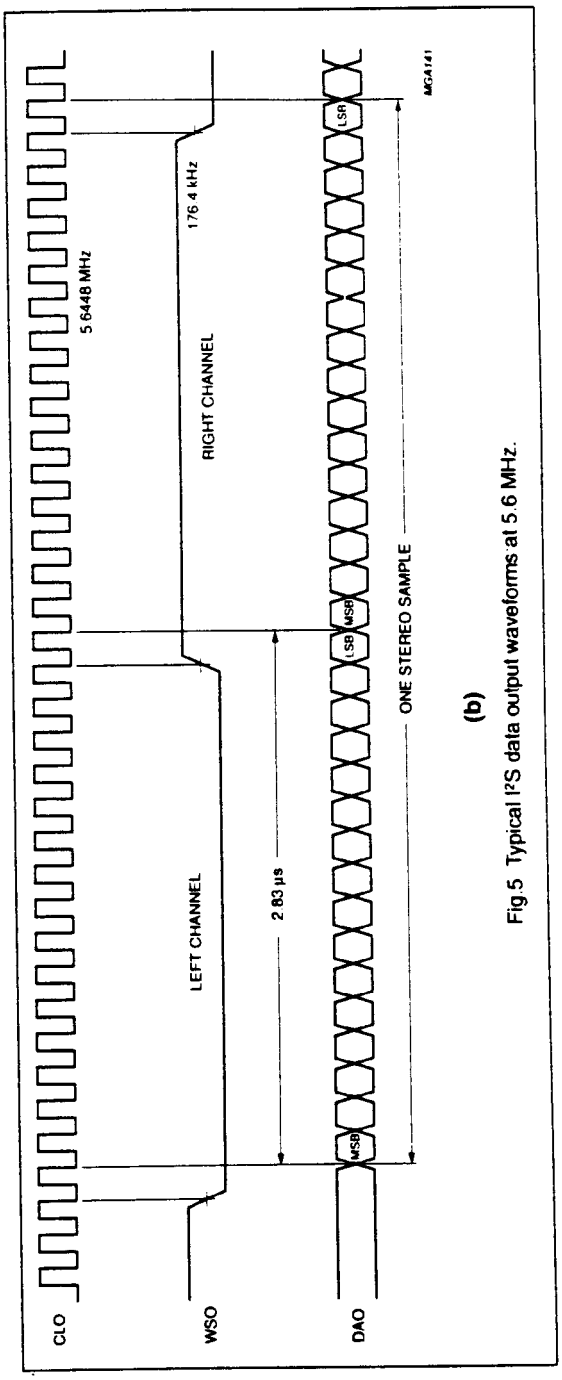
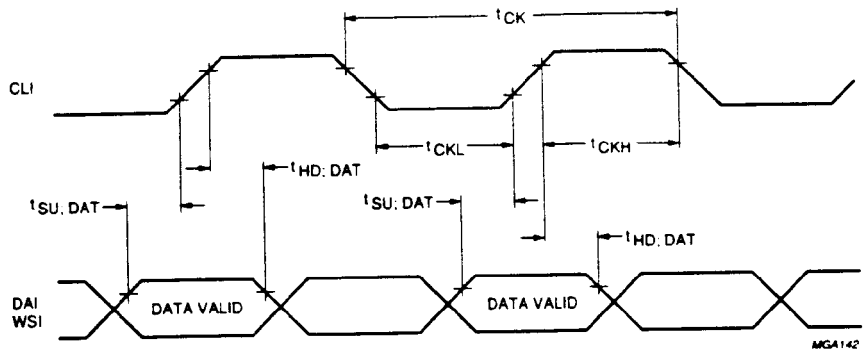
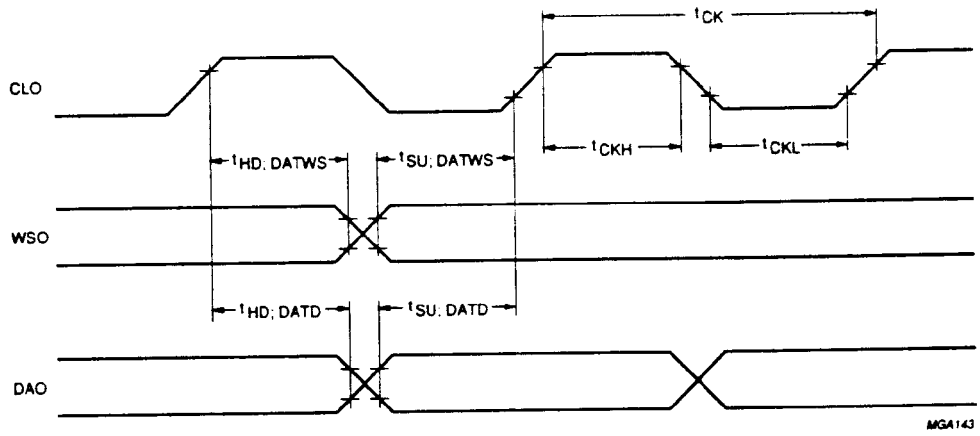


Fig.5 Typical I²S data output waveforms at 5.6 MHz.



Reference levels = 0.8 V and 2 V.

Fig.6 Data input timing with respect to I²S serial bit clock input (CLI).



Reference levels = 0.8 V and 2 V.

Fig.7 Data output timing with respect to clock output (CLO).

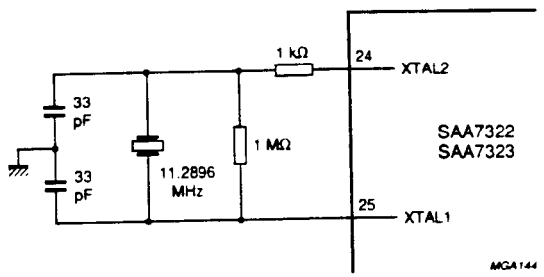


Fig.8 Crystal oscillator circuit using crystal type: 4322 143 05031.

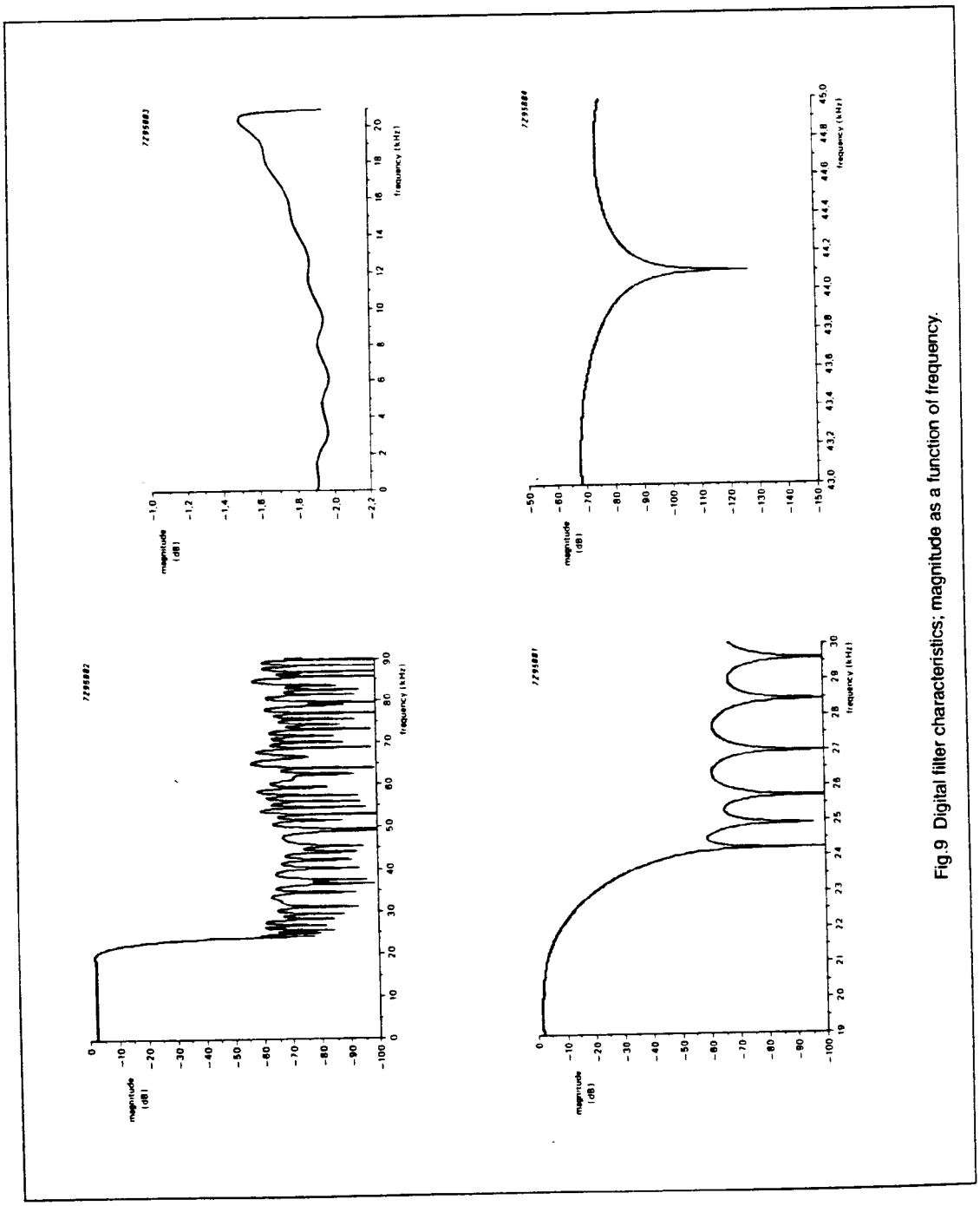


Fig.9 Digital filter characteristics; magnitude as a function of frequency.

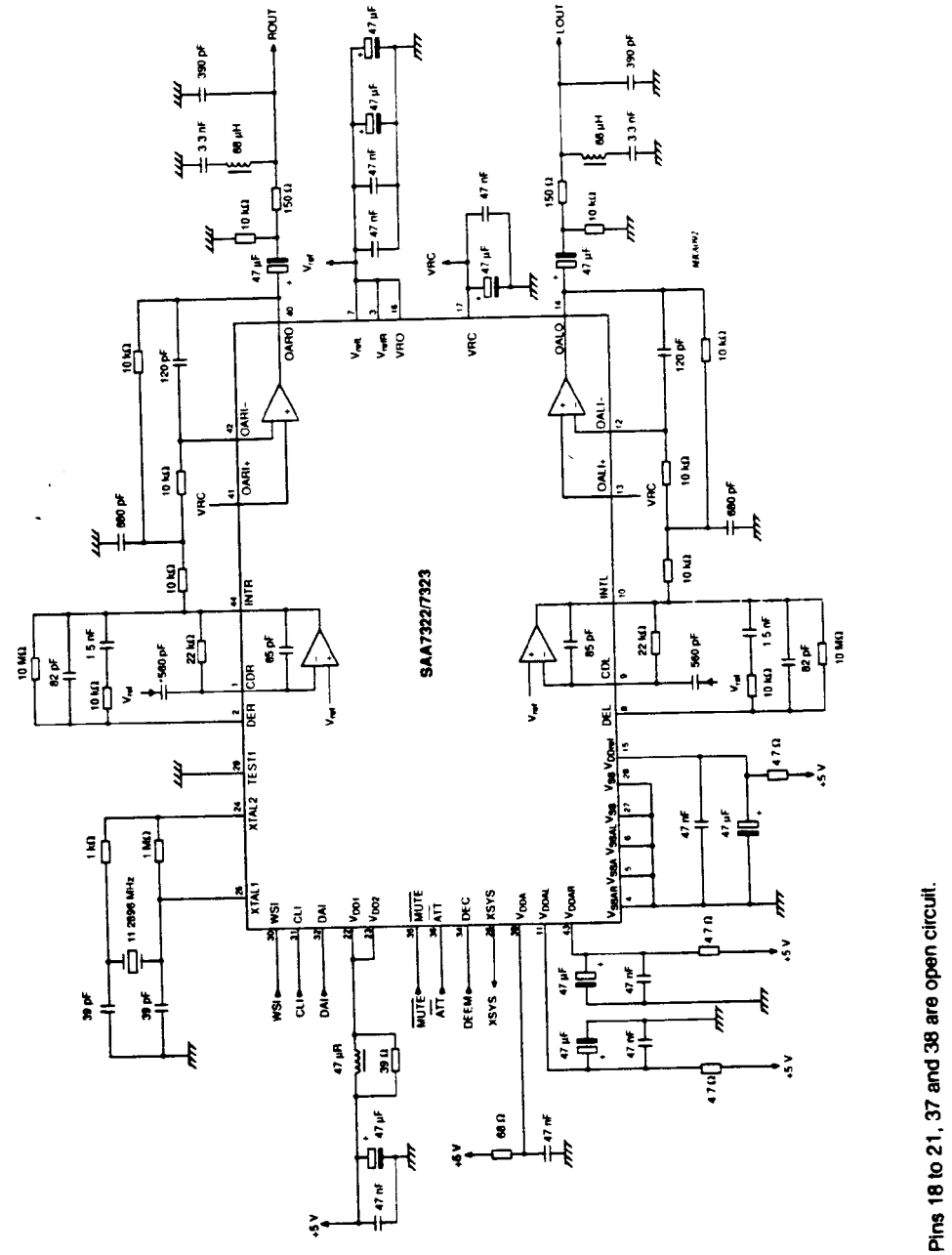


Fig.10 System application diagram.

Pins 18 to 21, 37 and 38 are open circuit.