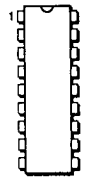
FEATURES

- ☐ Complete receiver in an 18-pin package
- ☐ Excellent performance
- ☐ CMOS, single 5 Volt operation

GENERAL DESCRIPTION

The SC11270/SC11271 are complete DTMF receivers integrating both the bandsplit filter and digital decoder functions. They are fabricated with Sierra Semiconductor's double-poly CMOS technology and are pin and function compatible with the MITEL, MT8870 and MT8870B-1 DTMF receivers, respectively. The filter section uses switched capacitor techniques for high- and low-group filters and dial tone rejection. Digital counting techniques are employed in the decoder to detect and decode all 16 DTMF tone-pairs into a 4 bit code. External component count is minimized by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface. The SC11271 conforms to CEPT specifications for DTMF receivers systems by providing a must reject signal level of –37 dBm.

18-PIN DIP PACKAGE



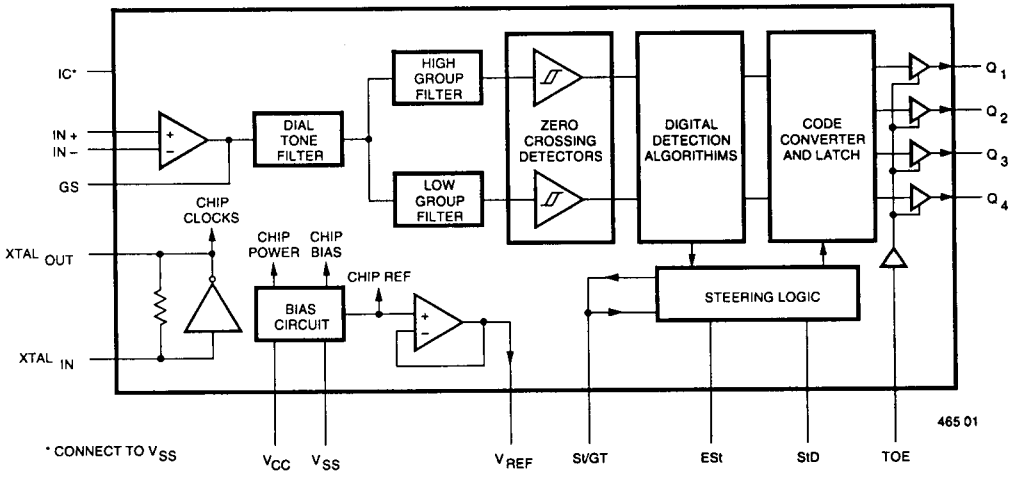
SC11270CN
SC11271CN
SC11270EN*
SC11721EN*

18-PIN SOIC PACKAGE

SC11270CM
SC11271CM
SC11270EM*
SC11271EM*

*Special order

BLOCK DIAGRAM



PIN DESCRIPTIONS

NAME	PIN	DESCRIPTION
ESt	16	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone-pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
GS	3	Gain Select. Gives access to output of front-end differential amplifier for connection of of feedback resistor.
IC	5, 6	Internal Connection. Must be tied to V_{SS}.
IN+	1	Non-Inverting Input — Connections to the front-end differential amplifier.
IN–	2	Inverting Input
OSC1	7	Clock Input — 3.579545 MHz crystal connected between these pins completes internal oscillator.
OSC2	8	Clock Output.
Q_1–Q_4	11–14	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see code table).
StD	15	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
St/GT	17	Steering input/guard time output (bi-directional). A voltage greater than VTS_t detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St (see truth table).
TOE	10	3-state output enable (input). Logic high enables the outputs Q_1–Q_4. Internal pull-up.
V_{CC}	18	Positive power supply, +5 V.
V_{REF}	4	Reference voltage output, nominally $V_{CC}/2$. May be used to bias the inputs at mid-rail (see application diagram).
V_{SS}	9	Negative power supply, normally connected to 0 V.

FUNCTIONAL DESCRIPTION

The SC11270/271 monolithic DTMF receivers offer small size, low power consumption and high performance. The architecture consists of a bandsplit filter section, which separates the high and low tones of a receiver pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two filters—a sixth order for the high group and an eight order for the low group. The bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see Figure 5). The filter section also incorporates notches at 350 Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second order switched-capacitor section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small

frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals ("third tones") and noise. When the detector recognizes the simultaneous presence of two valid tones (referred to as "signal condition" in some industry specifications), it raises the "early steering" flag (ESt). Any subsequent loss of signal-condition will cause ESt to fall.

Steering Circuit

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time-constant driven by ESt. A logic high on ESt causes V_C (see Figure 6) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone-pair, latching its corresponding 4-bit code (see Figure 3) into the output latch. At this point, the GT output is activated and drives V_C to V_{CC}. GT continues to drive high as long as ESt remains high. Finally after a short delay to allow the output latch to settle, the "delayed-steering" output flag, StD, goes high, signaling that a received tone-pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ("drop-out") too short to be considered a valid pause. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Figure 6 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 ms would be 300k.

Different steering arrangements may be used to select independently the guard-times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter-digital pause.

Guard-time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard-time adjustment is shown in Figure 7.

Input Configuration

The input arrangement of the SC11270 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 2 with the op-amp connected for unity gain and V_{REF} biasing the input at 1/2 V_{CC}. Figure 8 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

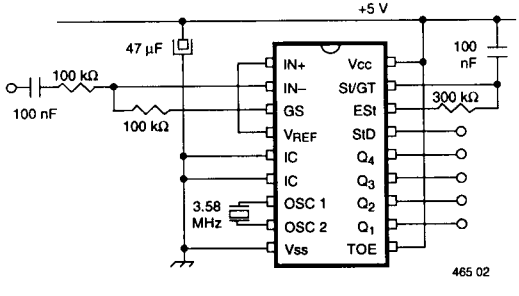
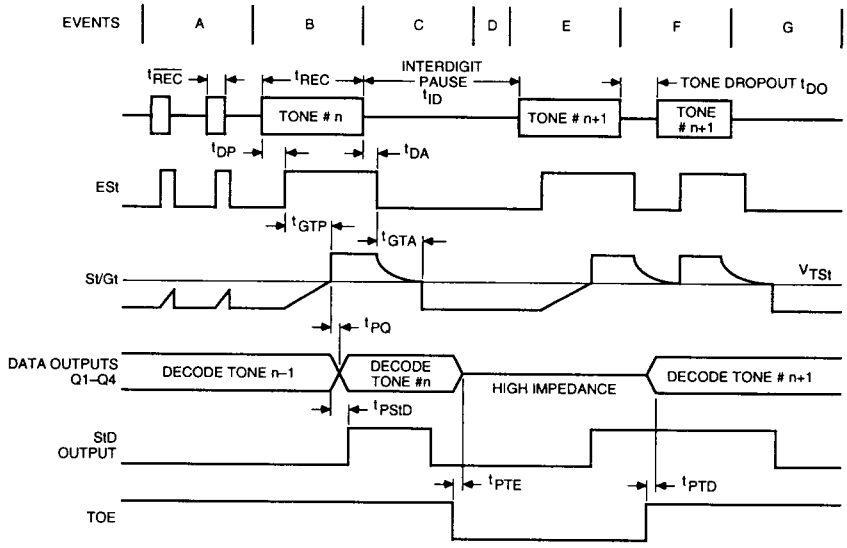


Figure 2. Single Ended Input Configuration

F_{low}	F_{high}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
–	–	ANY	L	Z	Z	Z	Z

"L = Logic Low, H = Logic High, Z = High Impedance"

Figure 3. Logic Table



A. Short tone bursts: detected. Tone duration is invalid.
B. Tone #n is detected. Tone duration is valid. Decoded to outputs.
C. End of tone #n is detected and validated.
D. 3 State outputs disabled (high impedance).
E. Tone #n+1 is detected. Tone duration is valid. Decoded to outputs.
F. Tristate outputs are enabled. Acceptable drop out of tone #n+1 does not register at outputs
G. End of tone #n+1 is detected and validated.

Figure 4. Timing Diagram

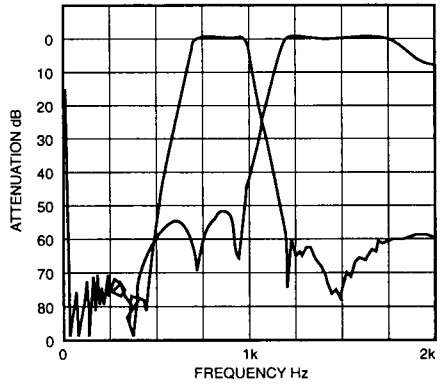


Figure 5. Typical Filter Characteristic

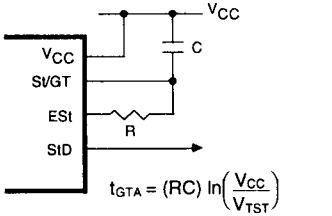


Figure 6. Basic Steering Circuit

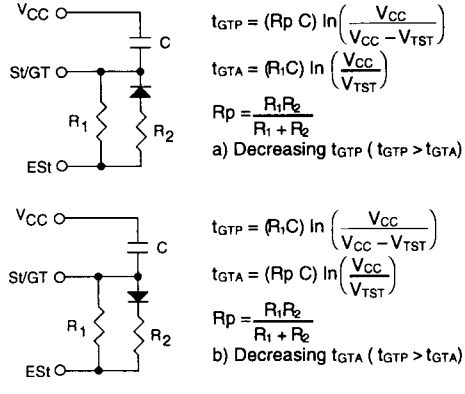


Figure 7. Guard Time Adjustment

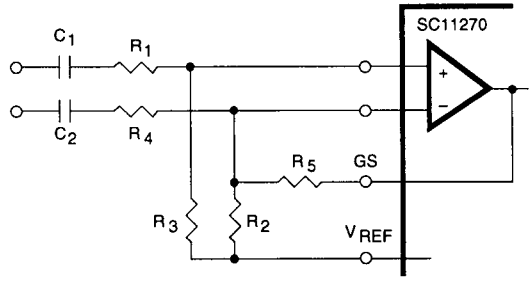


Figure 8 Differential Input Configuration

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC} – V_{SS}		+6 V
Voltage on any Pin		V_{SS} – 0.3 to V_{CC}+0.3 V
Current at any Pin		10 mA
Operating Temperature	SC11270, 11271EN, EM	-40 to +85°C
	SC11270, 11271CN, CM	0° to +70°C
Storage Temperature		-65 to +150°C
Power Dissipation (Note 3)		500 mW

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Unless otherwise specified, all voltages are referenced to ground.
NOTE 3: Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

DC ELECTRICAL CHARACTERISTICS (Notes 1 and 2)

PARAMETER	DESCRIPTION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY							
V_{CC}	Operating Supply Voltage			4.75		5.25	V
I_{CC}	Operating Supply Current				3.0	7	mA
P_O	Power Consumption		f=3.579 MHz; V_{CC}=5 V		15	35	mW
INPUTS							
V_{IL}	Low Level Input Voltage					1.5	V
V_{IH}	High Level Input Voltage			3.5			V
I_{IH}/I_{IL}	Input Leakage Current		V_{IN}=V_{SS} or V_{CC}		0.1		µA
I_{SO}	Pull Up (Source) Current		TOE (Pin 10)=0 V		7.5	15.0	µA
R_{IN}	Input Impedance	Signal Inputs 1, 2	@ 1 kHz		10		MΩ
V_{TSI}	Steering Threshold Voltage				2.35		V
OUTPUTS							
V_{OL}	Low Level Output Voltage		No Load		0.03		V
V_{OH}	High Level Output Voltage		No Load		4.97		V
I_{OL}	Output Low (Sink) Current		V_{OUT}=0.4 V	1.0	2.5		mA
I_{OH}	Output High (Source) Current		V_{OUT}=4.6 V	0.4	0.8		mA
V_{REF}	Output Voltage	V_{REF}	No Load	2.4		2.7	V
R_{OR}	Output Resistance				10		kΩ

OPERATING CHARACTERISTICS

Gain Setting Amplifier

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_N	Input Leakage Current	$V_{SS}<V_{IN}<V_{CC}$		±100		nA
R_{IN}	Input Resistance			10		MΩ
V_{OS}	Input Offset Voltage			±25		mV
PSRR	Power Supply Rejection	1 kHz		60		dB
CMRR	Common Mode Rejection	$-3.0\ V<V_{IN}<3.0\ V$		60		dB
A_{VOL}	DC Open Loop Voltage Gain			65		dB
f_C	Open Loop Unity Gain Bandwidth			1.5		MHz
V_O	Output Voltage Swing	$R_L \geq 100\ k\Omega$ to V_{SS}		4.5		V_{PP}
C_L	Tolerable Capacitive Load (GS)			100		pF
R_L	Tolerable Resistive Load (GS)			50		kΩ
V_{CM}	Common Mode Range	No Load		3.0		V_{PP}

Notes: 1. All voltages referenced to V_{SS} unless otherwise noted.
2. $V_{CC} = 5.0\ V$, $V_{SS} = 0\ V$, $T_A = 25°C$.

AC ELECTRICAL CHARACTERISTICS

All voltages referenced to V_{SS} unless otherwise noted. $V_{CC} = 5.0\ V$, $V_{SS} = 0\ V$, $T_A = 25°C$, $F_{CLK} = 3.579545$ MHz, using test circuit of Figure 2.

PARAMETER	DESCRIPTION			MIN	TYP	MAX	UNITS	NOTES
SIGNAL CONDITIONS								
	Valid Input Signal Level (each tone of composite signal)	MIN				-29	dBm	1,2,3,5,6,9
						27.5	mV_{RMS}	1,2,3,5,6,9
		MAX		+1			dBm	1,2,3,5,6,9
				883			mV_{RMS}	
	Twist Accept Limit		Positive		10		dB	2,3,6,9
			Negative		10		dB	
NON-ACCEPT LEVEL				-37			dBm	1,2,3,4,5,9
	Freq. Deviation Accept Limit					±1.5% ±2 Hz	Nom.	2,3,5,9
	Freq. Deviation Reject Limit			±3.5%			Nom.	2,3,5
	Third Tone Tolerance				-16		dB	2,3,4,5,9,10
	Noise Tolerance				-12		dB	2,3,4,5,7,9,10
	Dial Tone Tolerance				+18		dB	2,3,4,5,8,9,10

AC ELECTRICAL CHARACTERISTICS

All voltages referenced to V_{SS} unless otherwise noted. V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = 25°C, F_{CLK} = 3.579545 MHz, using test circuit of Figure 2.

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS	NOTES
TIMING							
t_{DP}	Tone Present Detection Time		5	14	16	ms	Refer to Fig. 4
t_{DA}	Tone Absent Detection Time		0.5	4	8.5	ms	
t_{REC}	Tone Duration Accept				40	ms	(User Adjustable)
t_{REC}	Tone Duration Reject		20			ms	
t_{ID}	Interdigit Pause Accept				40	ms	Refer to "Guard Time Adjustment"
t_{DO}	Interdigit Pause Reject		20			ms	
OUTPUTS							
t_{PQ}	Propagation Delay (St to Q)			8	11	µs	TOE=V_{CC}
t_{PSED}	Propagation Delay (St to StD)			12		µs	
t_{QSED}	Output Data Set Up (Q to StD)			4.5		µs	
t_{PTE}	Propagation Delay (TOE to Q)	DISABLE		50	60	ns	R_L=10 kΩ
t_{PTD}		ENABLE		300		ns	C_L=50 pF
CLOCK							
f_{CLK}	Crystal/Clock Frequency		3.5759	3.5795	3.581	MHz	
C_{LO}	Clock Output (OSC2)	Capacitive Load			30	pF	

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms, Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2 Hz.
7. Bandwidth limited (3 kHz) Gaussian Noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest level frequency component in DTMF signal.