TBA920 · TBA920S

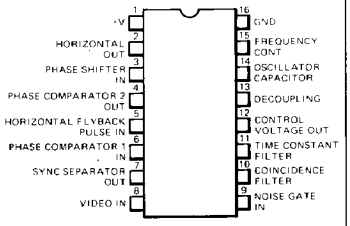
TELEVISION HORIZONTAL OSCILLATORS

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TBA920s are monolithic integrated circuits designed for TV receiver applications. They are constructed on a single silicon chip using the Fairchild Planar* process. They accept the composite video signal, separate sync pulses (with the added safeguard of noise gating) and provide a sync output for the vertical integrator. Also incorporated is the horizontal oscillator along with two phase comparators, one to compare flyback pulses to the oscillator and the other for sync phase comparison. The devices will interface with both SCR and transistor deflection systems.

- **SYNC SEPARATOR**
- **NOISE GATE**
- **HORIZONTAL OSCILLATOR**
- **DUAL PHASE COMPARATOR**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

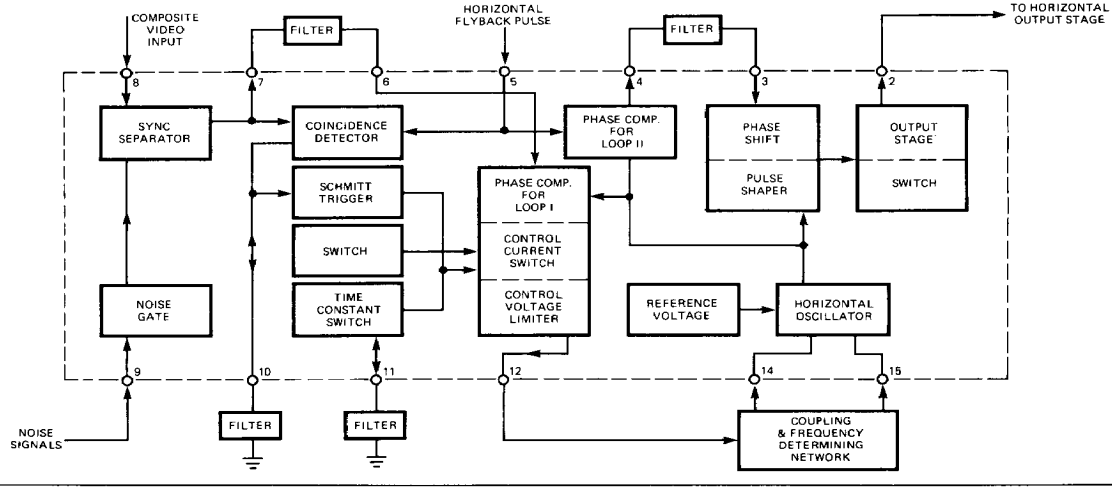
TYPE	PART NO.
920	TBA920
920S	TBA920S

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	13.2 V
Total Power Dissipation (Note 1)	600 mW
Storage Temperature	−55°C to +125°C
Operating Temperature	−20°C to +60°C
Pin Temperature (Soldering, 10 s)	260°C
Voltages	
V_{1-16}	13.2 V
V_{3-16}	0 to 13.2 V
V_{8-16}	−12 V
V_{10-16}	−0.5 to 5.0 V
Currents	
I_2 (Average Value)	−20 mA
I_2 (Peak Value)	−200 mA
I_5 (Peak Value)	10 mA
I_7 (Peak Value)	10 mA
I_8 (Peak Value)	10 mA
I_9 (Peak Value)	10 mA

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_{1-16} = 12V$, See Applications Circuit (CCIR Standard), unless otherwise specified.
***Note: TBA920S is identical to the TBA920 except as indicated.**

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Current Consumption	I_1	$I_2 = 0$		36		mA
Video Signal						
Input Voltage (Positive Going Sync) Peak-to-Peak Value	V_{IN} (p-p)		1.0	3.0	7.0	V
Input Current During Sync Pulse (Peak Value)	I_8			100		µA
Noise Gating (Lead 9)						
Input Voltage (Peak Value)	V_{9-16}		0.7			V
Input Current (Peak Value)	I_9		0.03		10	mA
Input Resistance	R_{9-16}			200		Ω
Flyback Pulse (Lead 5)						
Input Voltage (Peak Value)	V_{5-16}			±1.0		V
Input Current (Peak Value)	I_5		0.05	1.0		mA
Input Resistance	R_{5-16}			400		Ω
Pulse Duration	t_5	f = 15625 Hz	10			µs
Composite Sync Pulses (Positive, Lead 7)						
Output Voltage (Peak-to-Peak Value)	V_{7-16} (p-p)			10		V
Output Resistance						
at Leading Edge of Pulse (Emitter Follower)	R_{7-16}			50		Ω
at Trailing Edge	R_{7-16}			2.2		kΩ
Additional External Load Resistance	R_{7-16} (ext.)		2.0			kΩ
Driver Pulse (Lead 2)						
Output Voltage (Peak-to-Peak Value)	V_{2-16} (p-p)			10		V
Average Output Current	I_2 (AVG)				20	mA
Peak Output Current	I_2				200	mA
Output Resistance (Low Ohmic)	R_{2-16}	Note 2		2.5 or 15		Ω
Output Pulse Duration	t_2	Note 3		12 to 32		µs
Permissible Delay Between Leading Edge of Output Pulse and Flyback Pulse	t_d (tot)	$t_5 = 12$ µs		0 to 15		µs
Supply Voltage at Which Output Pulses are Obtained	V_{1-16}		4.0			V
Oscillator						
Frequency, Free Running	f_o	$R_{15-16} = 3.3$ kΩ (Note 4)		15625		Hz
Spread of Frequency at Nominal Values of Peripheral Components (TBA920)	$\frac{\Delta f_o}{f_o}$	Note 5			±5.0	%
*Spread of Frequency at Nominal Values of Peripheral Components (TBA920S)	$\frac{\Delta f_o}{f_o}$				±1.5	%
Frequency Change When Decreasing the Supply Down to Minimum 4.0 V	$\frac{\Delta f_o}{f_o}$				10	%
Frequency Control Sensitivity	$\frac{\Delta f_o}{\Delta I_{15}}$			16.5		Hz/µA
Adjustment Range of Network in Circuit on Application Information (TBA920)	$\frac{\Delta f_o}{f_o}$			±10		%
*Adjustment Range of Network in Figure 1 (TBA920S)	$\frac{\Delta f_o}{f_o}$			±5.0		%
Influence of Supply Voltage on Frequency	$\frac{\delta f_o/\delta V}{f_o/V_{nom}}$	$V_1 = 12$ V			5.0	%
Control Loop I (Between Sync Pulse and Oscillator)						
Control Voltage Range	V_{12-16}			0.8 to 5.5		V
Control Current (Peak Values)	I_{12}	$V_{10-16} > 4.5$ V; $V_{6-16} > 1.5$ V,		±2.0		mA
	I_{12}	$V_{10-16} > 2.0$ V; $V_{6-16} > 1.5$ V		±6.0		mA
Loopgain of APC System						
a. Time Coincidence Between Sync Pulse and Flyback Pulse or $V_{10-16} > 4.5$ V	$\frac{\Delta f}{\Delta t}$			1.0		kHz/µs
b. No Time Coincidence or $V_{10-16} < 2.0$ V	$\frac{\Delta f}{\Delta t}$			3.0		kHz/µs
Capture and Holding Range	Δf	Note 6		±1.0		kHz
Pull In Time for $\Delta f/f_o = \pm 3\%$	t	$\Delta f = 470$ Hz (Note 7)		20		ms
Switch Over From Large Control Sensitivity to Small Control Sensitivity After Capture	t	Note 7		20		ms

ELECTRICAL CHARACTERISTICS: (Cont'd)

CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
Control Loop II						
(Between Flyback Pulse and Oscillator)						
Permissible Delay Between Leading Edge of Output Pulse (Lead 2) and Leading Edge of Flyback Pulse	t_d (tot)			0 to 15		µs
Static Control Error	$\frac{\Delta t}{\Delta t_d}$	Note 8			0.5	%
Output Current During Flyback Pulse (Peak Value)	I_4			±0.7		mA
Overall Phase Relation						
Phase Relation Between Leading Edge of Sync Pulse and Middle of Flyback Pulse	t	Note 9		4.9		µs
Tolerance of Phase Relation (TBA920)	$\lvert\Delta t\rvert$	Note 10			1.0	µs
Tolerance of Phase Relation (TBA920S)	$\lvert\Delta t\rvert$				0.4	µs
Voltage for t_2 = 12 to 32 µs	V_{3-16}			6 to 8		V
Adjustment Sensitivity	$\frac{\Delta t_2}{\Delta V_{3-16}}$			10		µs/V
Input Current	I_3				2.0	µA
External Switch Over of Parameters (Loop Filter and Loop Gain) of Control Loop I (e.g. for Video Recorder Application) See Note 11						
Required Switch Over Voltage	V_{10-16}	R_{11-16} = 150 Ω	4.5			V
	V_{10-16}	R_{11-16} = 2.0 kΩ			2.0	V
Required Switch Over Current	I_{10}	R_{11-16} = 150 Ω, V_{10-16} = 4.5 V (Note 11)		80		µA
	I_{10}	R_{11-16} = 2.0 kΩ, V_{10-16} = 2.0 V (Note 11)		120		µA

NOTES:

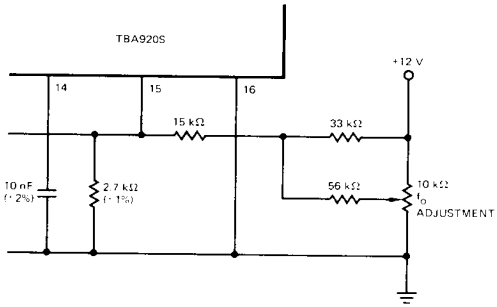
1. 800 mW permissible while tubes are heating up.
2. Depends on switch position and polarity output current. R_{2-16} = 2.5 Ω is valid for V_{2-16} = +10.5 V and a load between leads 2 and 16 (e.g. an external resistor).
3. The output pulse duration is adjusted by shifting the leading edge (V_{3-16} from 6.0 V to 8.0 V). The pulse duration is a result of delay in the line output device and the action of the second control loop in the TBA920.

   For a line output stage with BU108 high voltage transistor the resulting duration is about 22 µs, and in such a way that the line output transistor is switched on again about 8.0 µs after the middle of the line flyback pulse. This pulse duration must be taken into account when designing the driver stage and driver transformer as this way of driving the line output device differs from the usual, i.e. a driver duty cycle of about 50%.
4. The oscillator frequency can be changed for other TV standards by an appropriate value of C_{14-16}.
5. Exclusive external components tolerances.
6. Adjustable with R_{12-15}.
7. See application information circuit.
8. The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.
9. This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black and white sets), then the phase relation is achieved at C_{5-16} = 560 pF.
10. The adjustment of the overall phase relation and consequently the leading edge of the output pulse at lead 2 occurs automatically by the control loop II or by applying a dc voltage to lead 3.
11. With sync pulses at lead 7 and 8; without RC network at lead 10.

TEST CIRCUITS

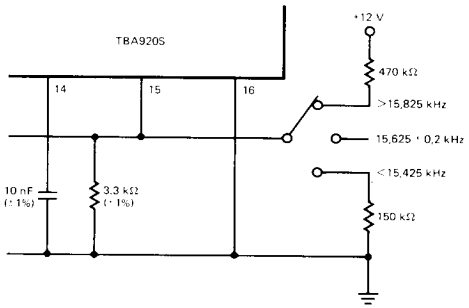
TBA920S

(See application circuit for balance of circuitry)



Frequency adjustment range. Test circuit for TBA920S.

Fig. 1



Other circuit possibilities for oscillator frequency adjustment.

Fig. 2

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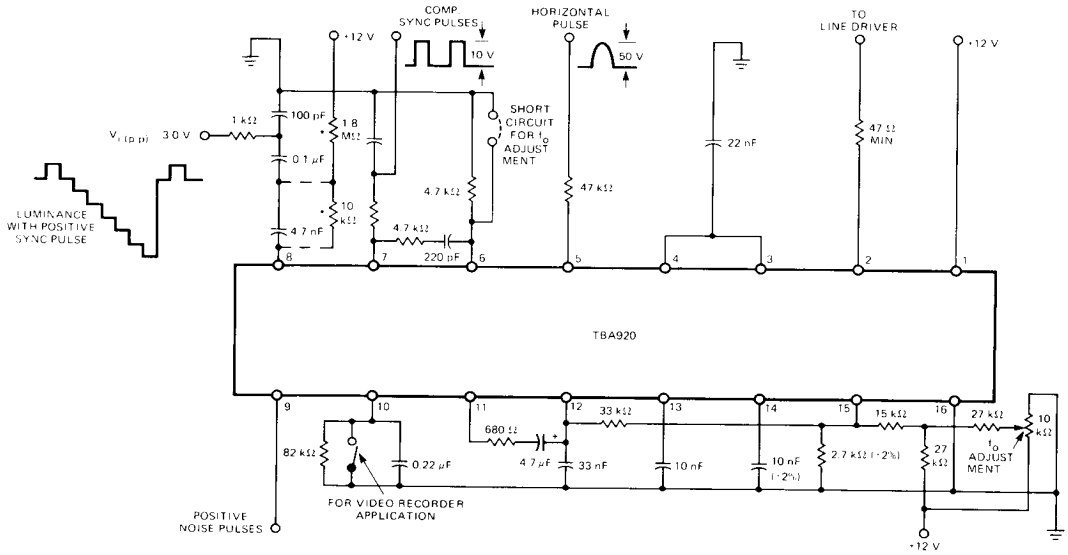
APPLICATION

(See Fig. 1 for TBA920S network)



*To bias input direct to base.