XR-2567 Dual Monolithic Tone Decoder

DESCRIPTION

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone-decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. A functional block diagram of the complete monolithic system is shown below. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

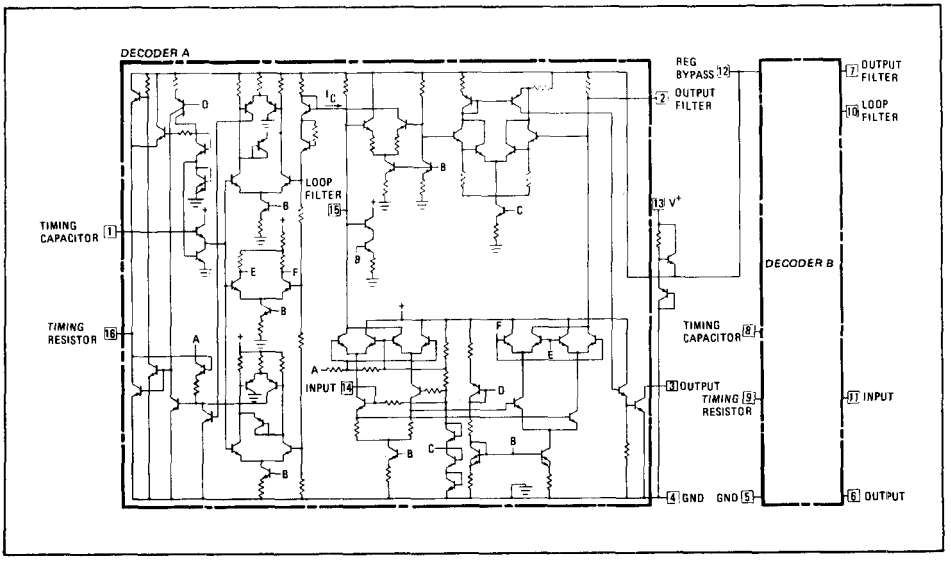
FEATURES

- *Replaces two 567-type decoders*
- Excellent temperature tracking between decoders
- Bandwidth adjustable from 0 to 14%
- Logic compatible outputs with 100 mA sink capability
- Center frequency matching (1% typical)
- Center frequency adjustable from 0.01 Hz to 500 kHz
- Inherent immunity to false triggering
- Frequency range adjustable over 20:1 range by external resistor

APPLICATIONS

- Touch-Tone® Decoding
- Sequential Tone Decoding
- Dual-Tone Decoding/Encoding
- Communications Paging
- Ultrasonic Remote-Control and Monitoring
- Full-Duplex Carrier-Tone Transceiver
- Wireless Intercom
- Dual Precision Oscillator
- FSK Generation and Detection

SCHEMATIC DIAGRAM



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ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, T_A = 25°C, unless otherwise specified.

Test circuit of Figure 1, S_1 closed unless otherwise specified.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
GENERAL					
Supply Voltage Range					
Without Regulator	See Figure 1, S_1 closed	4.75		7	Vdc
With Internal Regulator	See Figure 1, S_1 open	6.5		12	Vdc
Supply Current (both decoders)	See Typical Performance Data				
Quiescent XR-2567M	R_L = 20 KΩ		12	16	mA
XR-2567C	R_L = 20 KΩ		14	20	mA
Activated XR-2567M	R_L = 20 KΩ		22	26	mA
XR-2567C	R_L 20 KΩ		24	30	mA
Output Voltage				15	V
Negative Voltage at Input				-10	V
Positive Voltage at Input				V_{CC}+0.5	V
CENTER FREQUENCY*					
Highest Center Frequency		100	500		kHz
Center Frequency Stability					
Temperature T_A = 25°C	See Typical Performance Data		35		ppm/°C
0 < T_A < +75°C	See Typical Performance Data		±60		ppm/°C
-55° < T_A < +125°C	See Typical Performance Data		±140		ppm/°C
Supply Voltage					
Without Regulator XR-2567M	f_o = 100 kHz		0.5	1.0	%/V
XR-2567C	f_o = 100 kHz		0.7	2.0	%/V
With Internal Regulator XR-2567M	f_o = 100 kHz, V+ = 9V		0.05		%/V
XR-2567C	f_o = 100 kHz, V+ = 9V		0.1		%/V
DETECTION BANDWIDTH*					
Largest Detection Bandwidth XR-2567M	f_o = 100 kHz	12	14	16	% of f_o
XR-2567C	f_o = 100 kHz	10	14	18	% of f_o
Largest Detection Bandwidth Skew					
XR-2567M			1	2	% of f_o
XR-2567C			1	3	% of f_o
Largest Detection Bandwidth Variation					
Temperature	V_{in} = 300 mV rms		± 0.1		%/°C
Supply Voltage	V_{in} = 300 mV rms		± 2		%/V
INPUT*					
Input Resistance			20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, f_i = f_o		20	25	mV rms
Largest No-Output Input Voltage	I_L = 100 mA, f_i = f_o	10	15		mV rms
Greatest Simultaneous Outband Signal to Inband Signal Ratio			+6		dB
Minimum Input Signal to Wideband Noise Ratio	Noise Bw = 140 kHz		-6		dB
OUTPUT*					
Output Saturation Voltage	I_L = 30 mA, V_{in} = 25 mV rms		0.2	0.4	V
	I_L = 100 mA, V_{in} = 25 mV rms		0.6	1.0	V
Output Leakage Current			0.01	25	μA
Fastest ON-OFF Cycling Rate			fo/20		
Output Rise Time	R_L = 50Ω		150		ns
Output Fall Time	R_L = 50Ω		30		ns
MATCHING CHARACTERISTICS					
Center Frequency Matching	f_o = 10 kHz		1		%
Temperature Drift Matching	0°C < T_A < 75°C		±20		ppm/°C
	-55°C < T_A < 125°C		±50		ppm/°C

* Each decoder section.

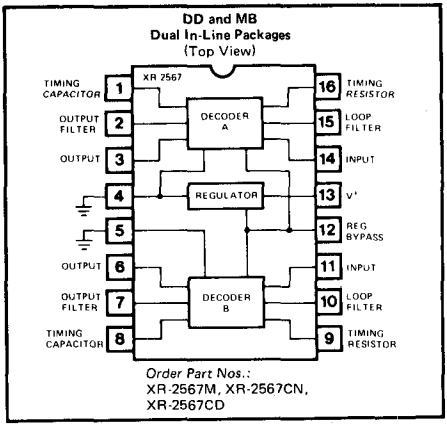
ABSOLUTE MAXIMUM RATINGS

Power Supply
- With Internal Regulator 14V
- Without Regulator (Pins 12 and 13 shorted) . . 10V

Power Dissipation
- Ceramic Package . . . . . 750 mW
- Derate above +25°C . . . . . 6 mW/°C
- Plastic Package . . . . . 625 mW/°C
- Derate above +25°C . . . . . 5 mW/°C

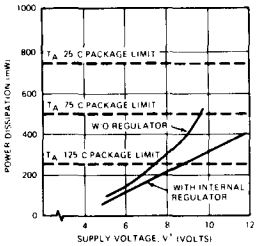
Temperature
- Operating: 2567M . . . . . -55°C to +125°C
- 2567C . . . . . 0°C to +75°C
- Storage . . . . . -65°C to +150°C

CONNECTION INFORMATION

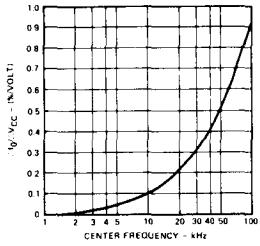


Order Part Nos.:
XR-2567M, XR-2567CN,
XR-2567CD

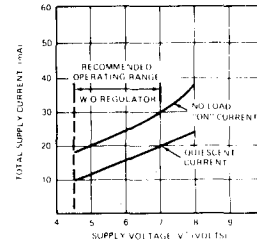
TYPICAL PERFORMANCE DATA



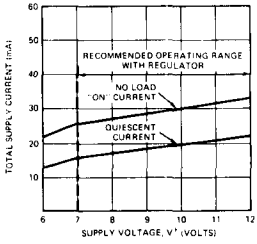
Internal Power Dissipation vs Supply Voltage. Both Units Activated, R_L = 20 K



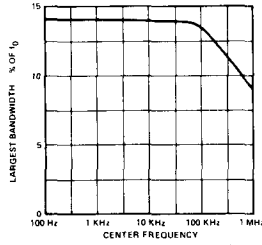
Power Supply Dependence of Center Frequency



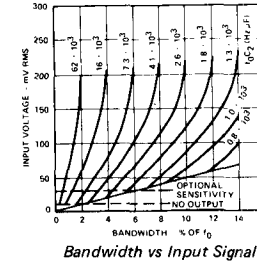
Total Supply Current vs Supply Voltage for Operation Without Internal Regulator (Pins 12 and 13 Shorted)



Total Supply Current vs Supply Voltage for Operation with Internal Regulator (Pins 12 and 13 Not Connected)



Largest Detection Bandwidth vs Operating Frequency



Bandwidth vs Input Signal Amplitude (C_2 in µF)

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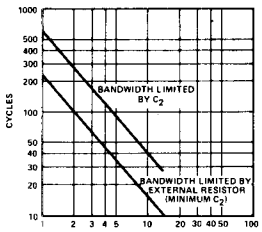
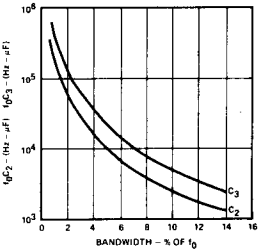
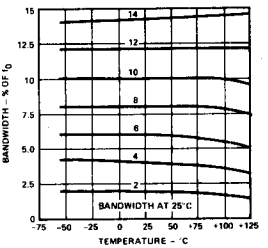
TYPICAL PERFORMANCE DATA (Cont)



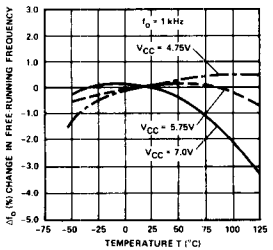
Greatest Number of Cycles Before Output



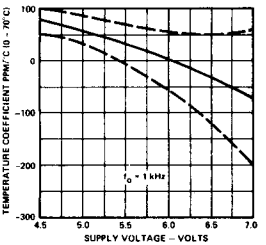
Detection Bandwidth as a Function of C_2 and C_3



Bandwidth Variation With Temperature



Frequency Drift With Temperature



Temperature Coefficient of Center Frequency (Mean and S.D.)

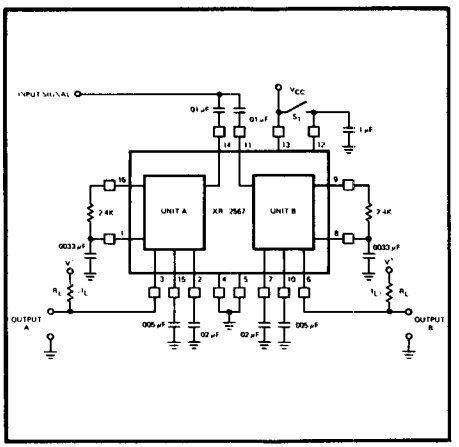
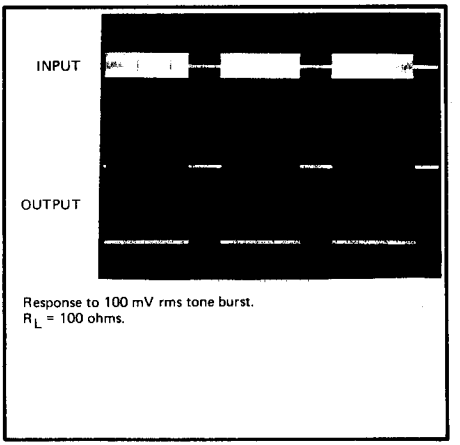


Figure 1. Test Circuit



Response to 100 mV rms tone burst.
R_L = 100 ohms.

Figure 2. XR-2567 Typical Response

DEFINITIONS OF THE XR-2567 PARAMETERS

The center frequency, f_0, is the *free-running frequency* of the current-controlled oscillator of the PLL with no input signal. It is determined by resistor R_1 and capacitor C_1; f_0 can be approximateed by

$$f_0 \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

The *detection bandwidth* is the frequency range centered about f_0, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a "logic zero" state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the lowpass bandwidth filter. The bandwidth of the filter, as a percent of f_0, can be determined by the approximation

$$BW \approx 1070 \sqrt{\frac{V_i}{f_0 C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance in μF at pins 10 or 15.

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency f_0. It is defined as $(f_{max} + f_{min} - 2f_0)/f_0$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

DESCRIPTION OF CIRCUIT CONTROLS

INPUT (PINS 11 AND 14)

The input signal is applied to pins 14 and/or 11 through a coupling capacitor, C_C. These terminals are internally biased at a dc level 2 volts above ground and they have an input impedance level of approximately 20 KΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (PINS 1, 8, 9, and 16)

The center frequency, f_0, of each decoder section is set by a resistor R_1 and a capacitor C_1. R_{1A} is connected between pins 1 and 16 in decoder section A, and R_{1B} between pins 8 and 9 of decoder section B. C_{1A} is connected from pin 1 to ground, and C_{1B} from pin 8 to ground, as shown in Figure 3. R_1 and C_1 should be selected for the desired center frequency by the expression $f_0 \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2 K$\Omega \leq R_1 \leq$ 20 KΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

For decoder section A, the oscillator output can be obtained at either pin 1 or 16. Pin 16 is the oscillator squarewave output which has a magnitude of approximately V_{CC}-1.4V and an average dc level of $V_{CC}/2$. A 1 KΩ load may be driven from this point. The voltage at pin 1 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 1 to avoid disturbing the temperature stability or duty cycle of the oscillator. For section B, pin 9 is the squarewave output and pin 8 the exponential triangle waveform output.

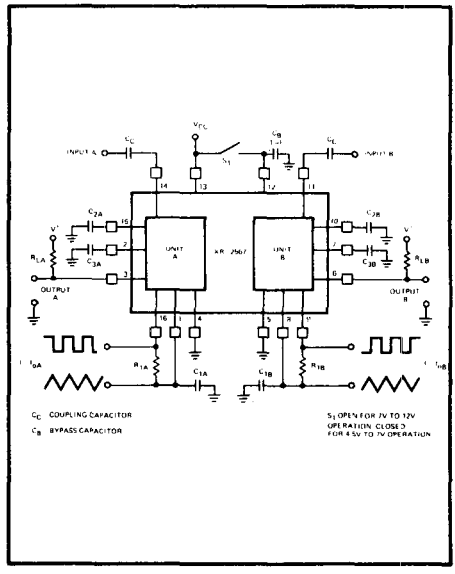


Figure 3. Circuit Connection Diagram

LOOP FILTER, C_2 (PINS 10 and 15)

Capacitors C_{2A} and C_{2B} connected from pins 15 and 10 to ground are the single-pole, lowpass filters for the PLL portion of decoder sections A and B. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 KΩ) is the impedance at pins 10 or 15. The selection of C_2 is determined by the detection bandwidth requirements and input signal amplitude as shown in the Curves. One approach is to select an area of operation from the graph and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_0C_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200$ mV rms. Then, as noted in the Curves, bandwidth will be controlled solely by the f_0C_2 product. (For additional information, see Optional Controls Section, "Speed of Response" and "Bandwidth Reduction".)

Pins 10 and 15 correspond to the PLL phase detector outputs of sections A and B, respectively. The voltage level at these pins is a linear function of frequency over the range of 0.95 to 1.05 f_0, with a slope of approximately 20 mV/% frequency deviation.

OUTPUT FILTER, C_3 (PINS 2 AND 7)

Capacitors C_{3A} and C_{3B} connected from pins 2 and 7 to ground form lowpass post detection filters for sections A and B respectively. The function of the post detection filter is to eliminate spurious outputs caused by out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3(4.7 K) is the internal impedance at pins 2 or 7.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, a minimum value for C_3 is $2C_2$, where C_2 is the loop filter capacitance for the corresponding decoder section. If C_3 is smaller than $2C_2$, then frequencies adjacent to the detection band may switch the output stage "off" and "on" at the beat frequency, or the output may pulse "off" and "on" during the turn-on transient.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, this delay may be desirable as a means of suppressing spurious outputs. (For additional information, see Optional Controls Section, "Speed of Response" and "Chatter".)

LOGIC OUTPUT (PINS 3 AND 6)

Output terminals 3 and 6 provide a binary logic output when an input signal tone is present within the detection-band of each respective decoder section. The logic outputs are uncommitted "bare-collector" power transistors capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L connected from V_{CC} to pins 3 and 6.

When an in-band signal is present, the output transistor at pins 3 or 6 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V^+ higher than the V_{CC} supply. For safe operation, $V^+ \leq 15$ volts.

REGULATOR BYPASS (PIN 12)

This pin corresponds to the output of the voltage regulator section. For circuit operation with a supply voltage greater than 7V, pin 12 should be ac grounded with a bypass capacitor $\geq 1\,\mu$F. For circuit operation over a supply voltage range of 4.5 to 7V, the voltage regulator section is not required; pin 12 should be shorted to V_{CC}.

GROUND TERMINALS (PINS 4 AND 5)

To eliminate parasitic interaction, each decoder section has a separate ground terminal. The internal regulator shares a common ground with decoder section A (pin 4).

Independent ground terminals also allow additional flexibility for split supply operation. Pin 4 can be used as V^-, and pin 5 as ground, as shown in Figure 4. When the circuit is operated with split supplies, the positive supply should always be >6V, and the dc potential across pins 13 and 14 should not exceed 15 volts.

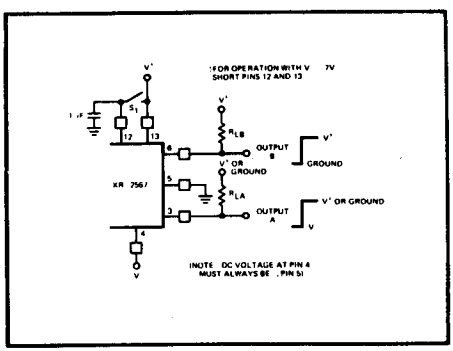


Figure 4. Split-Supply Operation Using Independent Ground Terminals of Units A and B. Unit A Operates Between V^+ and V^-, Unit B Operates Between V^+ and Ground

OPTIONAL CONTROLS

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus, maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_0/10$ Baud.

$$C_2 = \frac{130}{f_0}, \quad C_3 = \frac{260}{f_0}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 5 can be used to bring the quiescent C3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

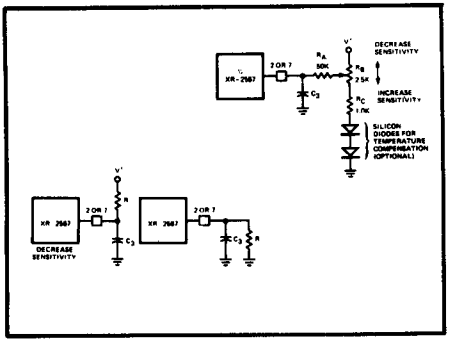


Figure 5. Optional Connections for Sensitivity Control

Although some loads, such as lamps and relays will not respond to chatter, "logic" may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input or by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

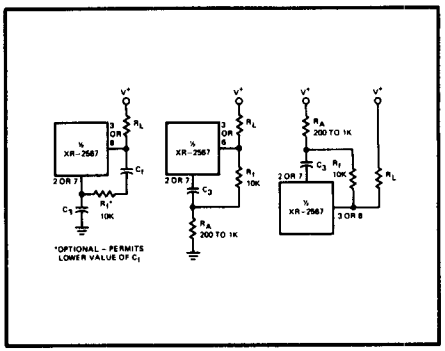


Figure 6. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Figure 7 can be used to change the position of the detection band (capture range) within the largest detection band (or loop range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

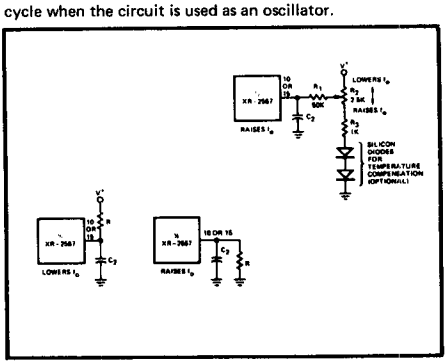


Figure 7. Connections to Reposition Detection Band

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OUTPUT LATCHING

After a signal is received, the output of either decoder section can be latched "on" by connecting a 20 KΩ resistor and diode from the "output" terminal to the "output filter" terminal as shown in Figure 8. The output stage can be unlatched by raising the voltage level at the output filter terminal.

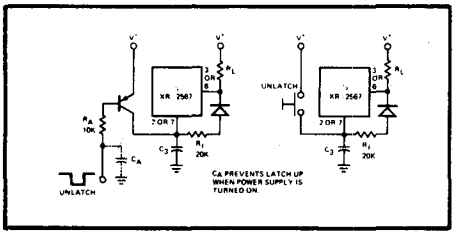
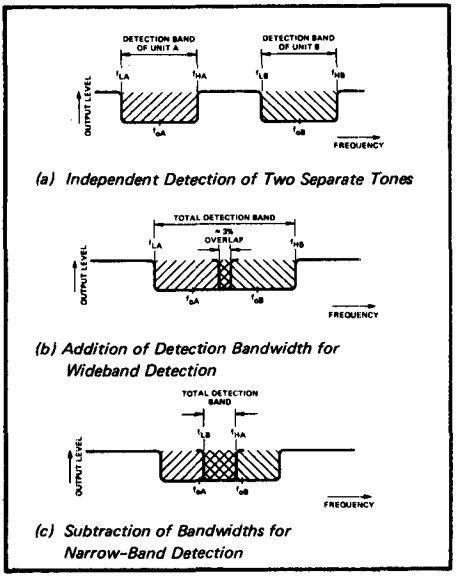


Figure 8. Output Latching

POSITIONING OF DETECTION BANDS

Figure 9 defines the respective band-edge and band-center frequencies for sections A and B of the dual tone decoder. Frequencies f_L and f_H with appropriate subscripts refer to the low and the high band-edge frequencies for decoder section A and B, and f_0 is the center frequency.



(a) Independent Detection of Two Separate Tones

(b) Addition of Detection Bandwidth for Wideband Detection

(c) Subtraction of Bandwidths for Narrow-Band Detection

Figure 9. Positioning of Detection Bands

The two sections can be interconnected to form a single-tone detector with an overall detection bandwidth equal to the sum of the difference of the detection bands for the two individual detector sections. For example, if the individual decoder sections are interconnected as shown in Figure 13, then the total detection bandwidth would be approximately equal to the sum of the respective bandwidths as shown in Figure 9 (b). Similarly, if the decoders are interconnected as shown in Figure 11, then the overall detection band would be equal to the difference, or the overlap, between the respective bandwidths as shown in Figure 9 (c).

BANDWIDTH REDUCTION

The bandwidth of each decoder can be reduced by either increasing the loop filter capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

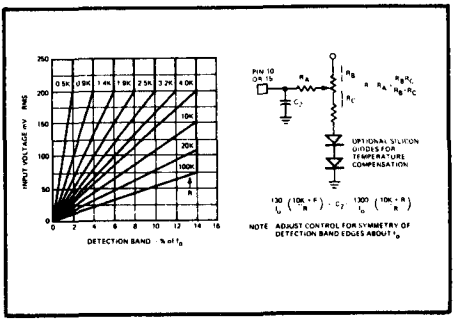


Figure 10. Bandwidth Reduction

Figure 10 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation.

Bandwidth reduction can also be obtained by subtracting over-lapping bandwidths of the two decoder sections (see Figures 9 (c) and 11).

APPLICATIONS

DUAL-TONE DETECTION

In most dual-tone detection systems, the decoder output is required to change state only when both input tones are present simultaneously. This can be implemented by setting the detection bandwidth of each of the XR-2567 decoder sections to cover one of the input tones; and then connecting the respective outputs through a NOR gate, as shown in Figure 11. In this case, the output of the NOR gate will be "high" only when both input tones are present simultaneously.

Figure 12 shows additional circuit configurations which can be used for decoding multiple-tone input signals. In Figure 12 (a), the output of Unit A is connected to the output filter (pin 7) of Unit B through the diode D_1. If no input tone is present within the detection-band of Unit A, then its output (pin 3) is "high", which keeps diode D_1 conducting and "disables" Unit B by keeping its output (pin 6) "high". If an input tone is present within the detection-band of Unit A, pin 3 is low, diode D_1 is reverse biased, and decoder B is no longer disabled. If under these conditions an input signal is present within the detection-band of Unit B, then its output at pin 6 would be "low". Thus, the output at pin 6 is "low" only when input tones within the detection-band of A and B are present simultaneously.

The dual-tone decoder circuit of Figure 12 (b) makes use of the split-ground feature of the XR-2567. The output terminal of Unit A is used as a "switch" in series with the ground terminal (pin 5) of Unit B. If the input tone A is not present, pin 3 is at its high-impedance state, and the ground terminal of Unit B is open-circuited. When the input tone A is present, pin 3 goes to a low-impedance state and Unit B is activated. In this manner, the output of Unit B will be "low" *only* when both tones A and B are present.

In the circuit connection of Figure 12 (b), Unit B does not draw any current until it is activated. Therefore, its power dissipation in a stand-by condition is lower than other dual-tone decoder configurations. However, due to finite series resistance between pin 3 and ground when Unit B is activated, the output current sink capability is limited to $\leqslant 10$ mA.

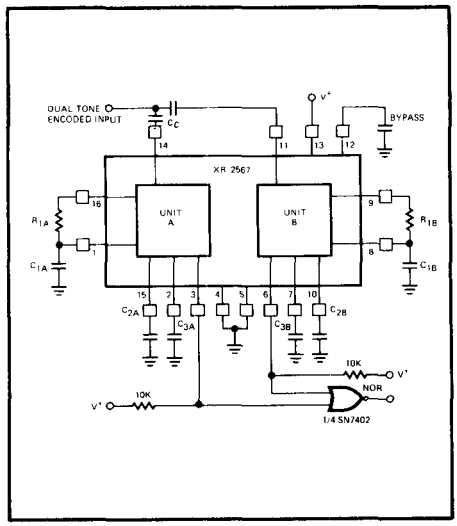


Figure 11. Connections for Decoding Dual-Tone Encoded Input Signals.

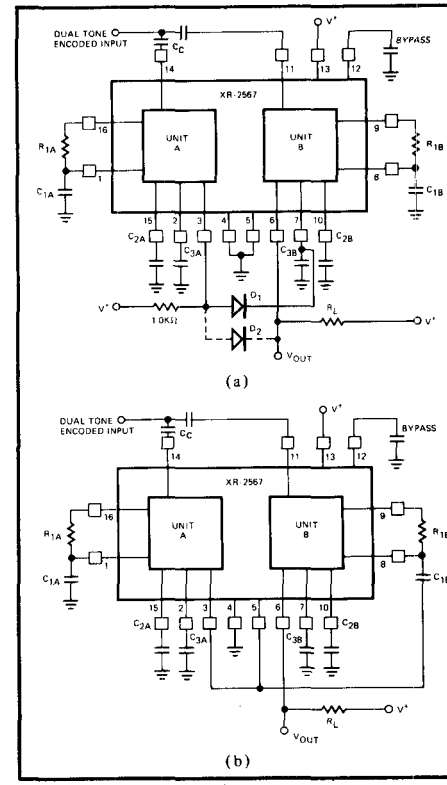


Figure 12. Additional Dual-Tone Decoding Circuits

SEQUENTIAL TONE DECODING

Dual-tone detector circuits can also be used for sequential tone decoding where one tone must be present before the other for the circuit to operate. This can be achieved by making the output filter capacitance, C_3, of one of the sections larger with respect to the other. For example, in the circuits of Figure 12 (a) and 13 (b), if C_{3A} is chosen to be much larger than C_{3B} ($C_{3A} \geqslant C_{3B}$), then Unit A will remain "on" and activate B for a finite time duration after tone A is terminated. Thus, the circuit will be able to detect the two tones only if they are present sequentially, with tone A preceding tone B.

The circuit of Figure 12 (a) can also be modified for sequential tone decoding by addition of a diode, D_2, between pins 3 and 6. Once activated by Unit A, Unit B will stay "on" as long as tone B is present, even though tone A may terminate. Once tone B disappears, the circuit is reset to its original state and would require tone A to be present for activation.

HIGH-SPEED NARROW-BAND TONE DECODER

The circuit of Figure 11 can be used as a narrow-band tone decoder by overlapping the detection bands of Units A and B (see Figure 9 (c)). The output of the NOR gate will be high only when an input signal is present within the overlapping portions of the detection band. To maintain uniform response within the passband, the input signal amplitude should be ⩾80 mV rms. For minimum response time, PLL filter capacitors C_{2A} and C_{2B} should be:

$$C_{2A} = C_{2B} \cong \frac{130}{f_0\,(\text{Hz})}\ \mu\text{F}$$

Under this condition, the worst-case output delay is ≈ 10 to 14 cycles of the input tone.

The practical matching and tracking tolerances of individual units limit the minimum bandwidth to ≈ 4% of f_0.

WIDEBAND DECODER

Figure 13 is a circuit configuration for increasing the detection bandwidth of the XR-2567 by combining the respective bandwidths of individual decoder sections. If the detection bands of each section are located adjacent to each other as shown in Figure 9 (b), and if the two outputs (pins 3 and 6) are shorted together, then the resulting bandwidth is the sum of individual bandwidths. In this manner, the total detection bandwidth can be increased to 24% of center frequency. To maintain uniform response throughout the passband, the input signal level should be ⩾80 mV rms, and the respective passbands of each section should have ≈3% overlap at center frequency.

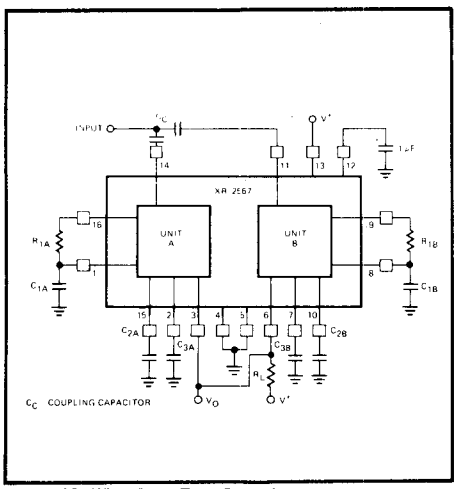


Figure 13. Wide-Band Tone Detection

TONE TRANSCEIVER

The XR-2567 can be used as a full-duplex tone transceiver by using one section of the unit as a tone detector and the remaining section as a tone generator. Since both sections operate independently, the circuit can transmit and receive simultaneously. A recommended circuti connection for transceiver applications is shown in Figure 14. In this case, Unit A is utilized as the receiver and Unit B is used as the transmitter. The transmitter section can be keyed "on" and "off" by applying a pulse to pin 8 through a disconnect diode D_1. The oscillator section of Unit B will be keyed "off" when the keying logic level at pin 8 is at a "low" state.

The output of the transmitter section (Unit B) can also be frequency modulated over a +6% deviation range by applying a modulation signal to pin 10.

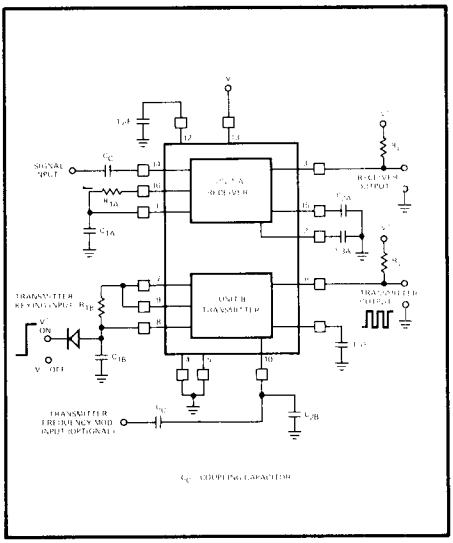


Figure 14. Tone Transceiver

HIGH CURRENT OSCILLATOR

The oscillator output of each section of XR-2567 can be amplified using the high current logic driver sections of the circuit. In this manner, each section of the circuit can switch 100 mA loads, without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 15. The oscillator frequency can be modulated over ±6% of f_0 by applying a control voltage to pins 15 or 10.

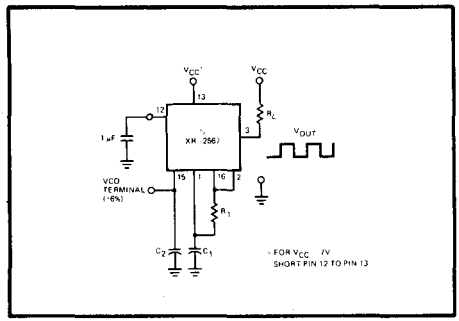


Figure 15. Precision Oscillator with High Current Output Capability

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2567M	Ceramic	-55°C to +125°C
XR-2567CN	Ceramic	0°C to +75°C
XR-2567CP	Plastic	0°C to +75°C