PLESSEY
Semiconductors

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# TBA950 : 2X

## LINE OSCILLATOR COMBINATION

The TBA950:2X is a monolithic integrated circuit for pulse separation and line synchronisation in TV receivers with transistor output stages.

The TBA950:2X comprises the sync. separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers prepared frame sync. pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration few external components are needed.

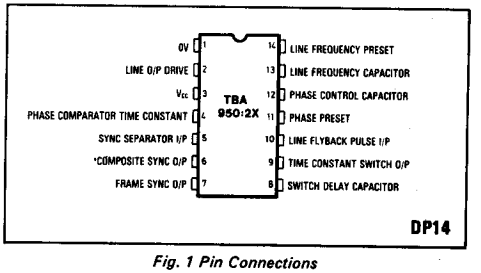


*Fig. 1 Pin Connections*

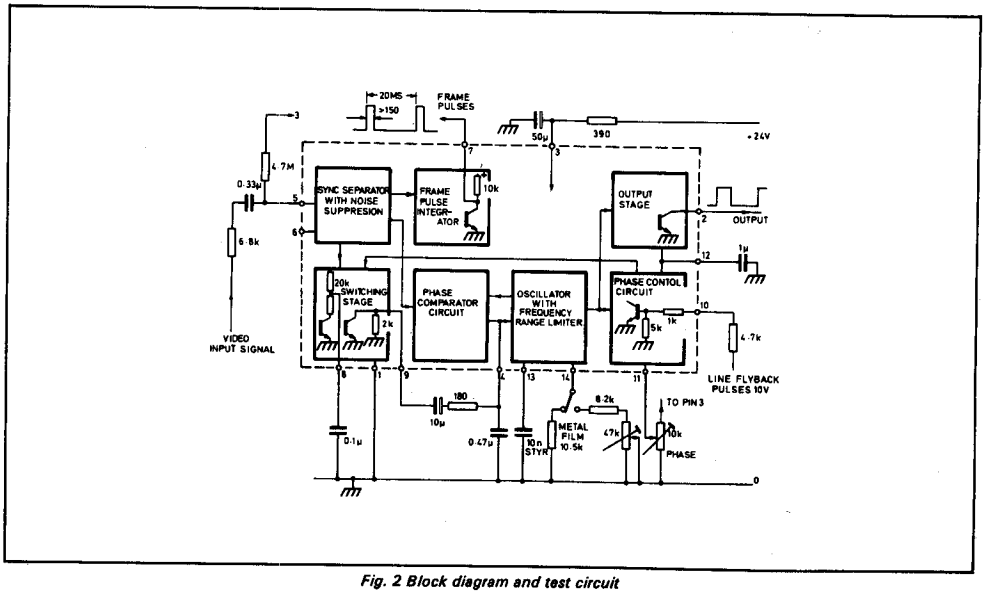


*Fig. 2 Block diagram and test circuit*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb} = +25°C$
$f_o = 15625Hz$ in the test circuit Fig.2 (see note 1)

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Amplitude of frame pulse | $V_1$ | | >8 | | V | |
| Frame pulse duration | $t_7$ | | >150 | | µs | |
| Output resistance at pin 7 (high state) | $R_{out\ 7}$ | 7.5 | 10 | 13 | kΩ | |
| Amplitude of sync. pulse | $V_6$ | | >8 | | V | |
| Output resistance at pin 6 | $R_{out\ 6}$ | 2.5 | | 4.5 | kΩ | |
| Output pulse duration | $t_2$ | 25 | | 28.5 | µs | Typical range |
| Residual output voltage | $V_{2\ res}$ | | <0.55 | | V | $I_2 = 20mA$ |
| Oscillator frequency | $f_o$ | 14843 | 15625 | 16406 | Hz | $C_{13/1} = 10nF$ $R_{14/1} = 10.5kΩ$ |
| Frequency pull-in range | $\pm \Delta f_F$ | 400 | | 1000 | Hz | Typical range |
| Frequency holding range | $\pm \Delta f_H$ | 400 | | 1000 | Hz | Typical range |
| Slope of phase comparator control loop | $df_o/dt_d$ | | 2 | | kHz/µs | |
| Gain of phase control | $dt_d/dt_p$ | | 20 | | | |
| Phase shift between leading edge of composite video signal and line flyback pulse (see note 2) adjustable by $V_{11}$ | $t_v$ | −1 | | 3.5 | µs | Typical range |

NOTES
1. By modification of the frequency-determining network at pins 13 and 14, these ICs can also be used for other line frequencies.
2. The limited flyback pulse should overlap the video signal sync. pulse on both edges.

## OPERATING NOTES

The sync. separator separates the synchronizing pulses from the composite video signal. The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync. pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network hitherto required between sync. separator and frame oscillator is no longer needed. Since the frame sync. pulse duration at pin 7 is subject to production spreads it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF polystyrene capacitor at pin 13 which is charged and discharged periodically by two internal current sources: The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync. pulses. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync. pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g. due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync. pulse on both edges (see Fig. 3).

The switching stage has an auxiliary function. When the two signals supplied by the sync. separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin. 9. Thus the time constant of the filter

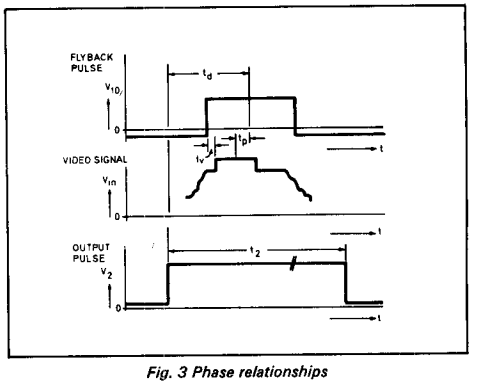


*Fig. 3 Phase relationships*

network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50Hz. This arrangement ensures disturbance-free operation.

For video recording operation this automaic switch-over can be blocked by a positive current fed into pin 8, e.g. via a resistor connected to pin 3. It may also be useful to connect a rsistor of about 630 Ω or 1 kΩ between pin 9 and earth. The capacitor at pin 4 may be lowered, e.g. to 0.1µF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e.g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to $V_3 = 4V$ and shuts off when $V_3$ falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as $V_3$ reaches 4.5V. In the range between $V_3 = 4.5V$ and full supply the shape and frequency of the output pulses are practically constant.

## RECOMMENDED OPERATING CONDITIONS

**For operating circuits Figs. 4 and 5**

| | |
|---|---|
| Input current during sync. pulse $I_5$ | $>5\mu A$ |
| Composite video input signal $V_{in\ p\text{-}p}$ | 3(1 to 6)V |
| Input current during line flyback pulse $I_{10}$ | 0.2 to 2 mA |
| Switchover current $I_8$ | $>2mA$ |
| Time difference between the output pulse at pin 2 and the line flyback pulse at 10, $t_d$ | $<20\mu s$ |
| Current consumption (see Fig. 6) $I_3$ | $<31mA$ |
| Ambient operating temperature range, $T_{amb}$ | 0 to +60° |

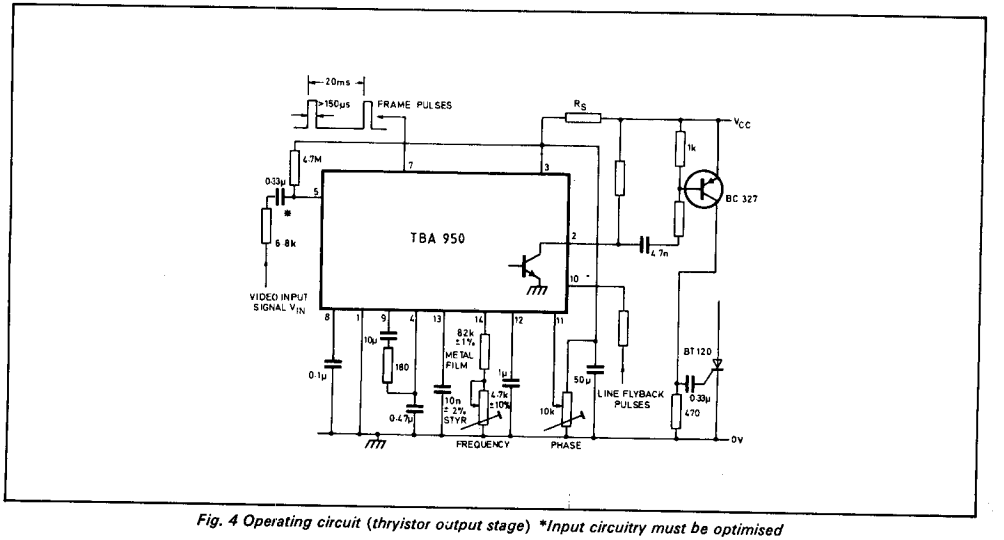


*Fig. 4 Operating circuit (thryistor output stage) *Input circuitry must be optimised*

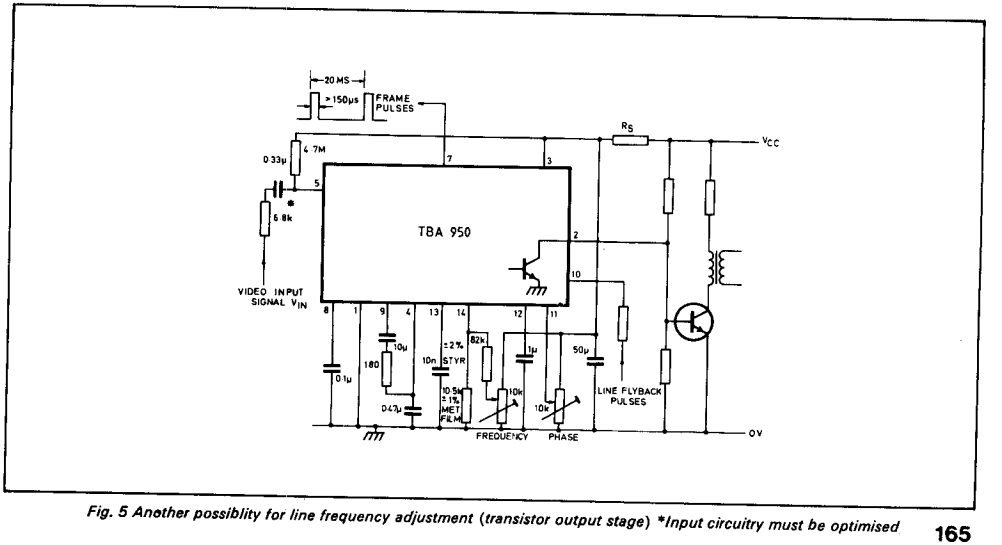


*Fig. 5 Another possiblity for line frequency adjustment (transistor output stage) *Input circuitry must be optimised*

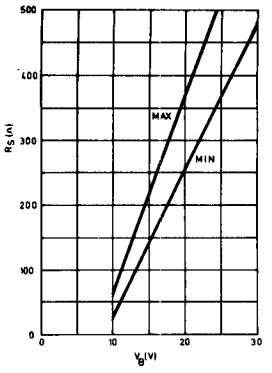


*Fig. 6 Graph for determining the supply series resistor $R_5$*

## ABSOLUTE MAXIMUM RATINGS

**All voltages are referred to pin 1**

| | |
|---|---|
| Supply current (see Fig. 6) $I_5$: | 45mA |
| Input current $I_5$: | 2mA |
| Input voltage $V_5$ | −6V |
| Output current $I_2$ | 22mA |
| Output voltage $V_2$: | 12V |
| Switch-over current for video recording $I_8$ | 5mA |
| Phase correction voltage $V_{11}$: | 0 to $V_3$ |
| Operating temperature range | −10°C to +60°C |
| Storage temperature range | −55°C to +125°C |